See columns 1, 4 o 5.

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: 0 268 492 A2

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 87310247.9

(51) Int. Cl.⁴: G 08 C 15/04

(22) Date of filing: 19.11.87

(30) Priority: 20.11.86 US 934238

(43) Date of publication of application:
25.05.88 Bulletin 88/21

(84) Designated Contracting States:
BE CH ES FR GB IT LI

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(54) A common bus multimode sensor system.

(57) A multinode noise immune sensor system that transmits AC power and returning sensor signals from remote units through a coaxial cable. An isolation transformer and an integrated circuit type pin programmable bus interface are also used. A carrier is provided by a ripple counter producing a frequency divided signal compared to a fixed reference frequency, where the result of the comparison controls a voltage-controlled oscillator, which produces a signal which is applied to the coaxial cable. Receivers at the end of the coaxial cable are each tunable to a designated carrier frequency and each decode the respective encoded signal.

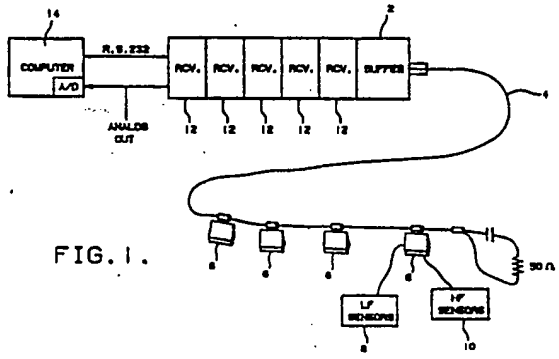

FIG. 1.

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Description

A COMMON BUS MULTINODE SENSOR SYSTEM

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention is directed to a common bus multinode sensor system that allows multiple remote units to simultaneously transmit over the common bus using frequency division multiplexing and, more particularly, to a system that provides power to the remote units via the bus and allows low speed digital, low frequency analog signals and high frequency analog signals to be transmitted over the bus to receivers which demodulate the analog signals and decode the digital signals.

Description of the Related Art

Closed loop communication systems for facilities such factories and nuclear power plants require the capability of transmitting digital, low frequency analog and high frequency analog signals from a plurality of spaced apart points to a central location through an environment full of electromagnetic noise. Such systems typically require that the communication medium such as a twisted wire pair, coaxial cable or optical light guide be spread out through a very large complex requiring a media up to two kilometers in length. Prior art methods of providing such closed loop networks typically provide synchronous data transmission over a transmit channel and a receive channel. These systems poll each remote unit separately and, as a result, operate using a time division multiplexing scheme. The use of time division multiplexing does not allow plural sensors to be sampled simultaneously. The prior art systems also require power supplies at each remote unit producing ground loop problems as well as requiring that extra power wires be provided to the remote units.

SUMMARY OF THE INVENTION

The present invention provides a communications system that allows slow speed digital as well as low frequency and high frequency analog signals to be simultaneously transmitted for a plurality of sensors. Preferably, the communications system sends power remote units over a common bus, provides a remote unit that can interface plural types of sensors, provides separate communication channels for each remote unit, allows plural low speed analog signals to be multiplexed, provides a low cost remote unit that takes advantage of medium scale integration, allows asynchronous data collection, allows each remote unit to be flexibly assigned different channel frequencies for communication, and allows easy addition of remote units.

The invention in its broad form resides in a common bus multinode sensor system for at least one sensor to convey a sensor signal, comprising a power supply, a communication cable coupled to and carrying said power supply, remote sensor means, coupled between said cable, and said sensor, characterized by means providing a carrier and for frequency-division multiplexing the sensor signal onto said cable and receiving power from said cable; and receiver means, coupled to said cable, for demultiplexing the frequency division multiplexed sensor signal.

Described hereinafter is a multinode system that transmits power down a common bus coaxial cable typically using an alternating current power source. Each remote unit connected to the coaxial cable converts the alternating current power to direct current power for an integrated circuit bus interface. The interface is externally pin programmable to provide a carrier at a frequency for a channel assigned to the remote unit thereby providing each remote unit with an individual identity. When plural low frequency analog signals are to be transmitted over the common bus, an on-chip multiplexer multiplexes the signals to an off-chip, external analog-to-digital converter. The analog-to-digital converter loads an on-chip parallel-to-serial out-shift register that applies each bit of the digitized signal serially to an on-chip Manchester encoder. The encoder modifies the input voltage of an on-chip voltage-controlled oscillator operating at the carrier frequency. The modulated frequency oscillator signal is applied to the coaxial cable. Receivers at the end of the coaxial cable can be tuned to the designated carrier frequencies to demodulate and then decode the encoded signal at any time. If a high frequency analog signal is supplied, it is used to directly modify the voltage applied to the voltage-controlled oscillator; that is, the carrier frequency is modulated by the high frequency signal and the receiver operating at the carrier frequency demodulates the signal. The integrated circuit is arranged so that the digital circuitry is generally isolated from and on the opposite side of the chip from the analog circuitry so noise immunity is enhanced. The digital and analog circuitry have separate power supplies. The circuit is arranged in a carrier so that critical lead wire runs are held to a minimum.

BRIEF DESCRIPTION OF THE DRAWINGS

A more detailed understanding of the invention can be had from the following description of a preferred embodiment, given by way of example and to be studied in conjunction with the accompanying drawing, wherein

Figure 1 illustrates a multinode system in accordance with the present invention;

Figure 2 illustrates the components of one of the remote units 6 of Fig. 1;

Figure 3, including Figs. 3A and 3B, illustrates the ripple counter 32 and decoder 38 of Fig. 2;

Figure 4 illustrates one of the reset flip-flops of Fig. 3;

Figure 5 illustrates the details of the phase/frequency comparator 34 of Fig. 2;

Figure 6 illustrates the details of the oscillator 42 of Fig. 2;

Figure 7, including Figs. 7A and 7B, illustrates the details of the timing counters 40 of Fig. 2, including timing signal buffers;

Figure 8 illustrates one of the D flip-flops of Fig. 7;

Figure 9 illustrates one of the asynchronous set D flip-flops of Fig. 7;

Figure 10 depicts the details of the analog multiplexer 46 of Fig. 2;

Figure 11, including Figs. 11A and 11B, illustrates the details of the latch 50 and shift register 52 of Fig. 2;

Figure 12 illustrates the details of the single bit latches of Fig. 11;

Figure 13 depicts the dual input D flip-flop of Fig. 11;

Figure 14, including Figs. 14A and 14B, depicts the timing diagram for the integrated circuit 30, particularly illustrating the timing relationship to the external analog-to-digital converter 48 of Fig. 2;

Figure 15 illustrates the details of the Manchester encoder 54 of Fig. 2;

Figure 16, including Figs. 16A and 16B, illustrates the timing of the Manchester encoder 54 for example data;

Figure 17 illustrates the details of the loop filter amplifier 58 of Fig. 2;

Figure 18 illustrates the details of the voltage-controlled oscillator 36 of Fig. 2;

Figure 19 illustrates a typical level shift circuit which allows the inputs to the integrated circuit 30 of Fig. 2 to match the signal requirements of the circuit 30;

Figure 20 illustrates a composite mask of the integrated circuit 30 of the present invention;

Figure 21, including Figs. 21A and 21B, depicts the layout of the mask;

Figure 22 illustrates the components of the buffer 2 and receivers 12 of Fig. 1;

Figure 23 is a conceptual block diagram of the process performed by the microcomputer 660 of Fig. 22;

Figure 24, including Figs. 24A-24F, illustrates the process of Fig. 23 in greater detail;

Figure 25 illustrates the details of the frequency synthesizer update subroutine called from Fig. 24;

Figure 26 illustrates the details of the send subroutine called from Fig. 24;

Figure 27, including Figs. 27A and 27B, illustrates the functions performed by the interrupt routine of the microcomputer 660 of Fig. 22; and

Figure 28, including Figs. 28A-28C, illustrates the interrupt routine in greater detail.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention provides an improved sensor system that allows up to 128 remote sensor units to asynchronously and simultaneously transmit data over a common coaxial cable to a distantly located receiver and computer and receive power via the same cable. A buffer board 2, as illustrated in Fig. 1, preferably supplies alternating current power to a coaxial cable 4 which has remote units 6 attached thereto; however, the power supplied could be direct current. The cable can be a standard 1/4 or 1/2 inch 50 ohm cable. Each of the remote units 6 converts the alternating current power carried by the coaxial cable 4 to direct current to power an analog serial bus interface and other node components. The interface integrated circuit can sample low frequency sensors 8, encode the sensor signals and transmit same over the coaxial cable 4 on a designated frequency channel. Each remote unit 6 is assigned a different carrier frequency. The interface can also transmit signals from a high frequency sensor 10 over the cable 4 in the designated channel. The frequency division multiplexed signal produced by each remote sensor unit 6 is demodulated by an appropriate receiver 12 which can be tuned to the designated channel frequency. If the sensor signals have been encoded, the respective receiver 12 also decodes the sensor signals and supplies same to the computer 14. The computer 14 would normally be a sophisticated, high speed process control-type machine; however, a simple IBM PC is acceptable. If the high frequency sensor signal is transmitted by the remote unit 6, the respective receiver 12 produces same as analog output signal.

As illustrated in Fig. 2, a common transformer 26 couples the alternating current, at, for example, 28 volts and 60 Hz, to a power supply 28 which converts the alternating current into positive and negative direct current supplied to an analog serial bus interface integrated circuit 30. The transformer 26 also provides isolation preventing the failure of a single node from knocking out the entire system. The power supply is a common power supply which will convert a 60-cycle, 28-volt signal into plus 5 volt, minus 5 volt and ground direct current sources and supply at least 100 milliwatts, the minimum necessary for the interface 30, but preferably at least one watt so that other circuits and sensors can be adequately powered. It is also possible to construct a simple power supply from two diodes, two capacitors and three terminal regulators available from National Semiconductor as described in the National Semiconductor Linear Databook, 1982, in the application hints on pages 1-20.

The interface 30 includes a ripple counter 32 which receives a multibit frequency designation word from programming pins external to the chip 30. The multibit frequency designation word designates the carrier frequency assigned to the particular remote unit 6. The ripple counter 32 is reloaded with the frequency selection word from the external pins each time the decoder 38 detects a count of zero. The phase/frequency comparator 34 compares the ripple counter carry-out signal to a reference frequency of approximately 44.7 kilohertz from timing counters 40. The timing counters 40 also produce timing signals for other devices on the chip 30. The timing counters 40 are driven by an oscillator 42 connected to an external oscillator crystal 44 such as a TV crystal which oscillates at approximately 3.5 megahertz. The ripple counter 32,

decoder 38, phase/frequency comparator 34, voltage-controlled oscillator 36, timing counters 40 and oscillator 42 create a programmable frequency synthesizer that operates off of a crystal reference such as the TV crystal.

The timing counters 40 also control the multiplexing of low frequency analog sensors 22 by an analog multiplexer 46. The analog multiplexer 46 provides the analog signals from one of the sensors 22 to an external analog-to-digital converter 48 available from G.E. Intersil as a 7109 converter. the sample rate of the converter 48 is controlled by a timing signal from the timing counters 40. When the analog-to-digital converter 48 has converted the selected analog signal, the digital value thereof is stored in latch 50. When the prior contents of shift register 52 have been shifted out, the contents of latch 50, as well as a two-bit address from the analog multiplexer 46, are loaded in parallel into the shift register 52. The two-bit address from the multiplexer 46 indicates which of the four analog signals is currently being sampled. The shift register 52 then serially outputs its contents to a Manchester encoder 54. The Manchester encoder 54 modifies the voltage produced by a filter 56 applied to the voltage-controlled oscillator 36. The chip 30 also includes a loop filter amplifier 58, is used for filtering out high frequency components.

During operation, the phase/frequency comparator 34 drives the voltage produced by the filter 56 upward whenever the voltage-controlled oscillator 36 is producing a frequency lower than the carrier frequency and drives the voltage downward whenever the voltage-controlled oscillator frequency is higher than the carrier frequency, and tends to track the carrier frequency designated by the inputs to the ripple counter 32. As a result, the Manchester encoder 54 is frequency shift keying the signal produced by the volage-controlled oscillator 36 by raising or lowering the voltage produced by the filter 56 in dependence upon the signal output by the Manchester encoder 54. The output of the voltage-controlled oscillator 36 is coupled to the coaxial cable 4 through a transformer 60. The transformer should be a high frequency transformer capable of operating in the 6 to 12 megahertz frequency range. Such a transformer can be constructed by winding several turns of wire around a ferrite core and providing an isolation resistor of 5k ohms.

As can be seen from the above discussion, the interface chip 30 encodes the analog signals and modulates a carrier frequency therewith. As a result, it is possible for the chip 30 to sample and transmit the values for four low frequency analog sensors 22. If a high frequency analog input signal, such as a signal from a piezosensor (up to 20 kHz with a dynamic range of 70 dB), is to be transmitted, the high frequency signal directly modulates the voltage produced by filter 56 so that the output of the voltage-controlled oscillator 36 is a carrier frequency modulated by the high frequency analog input signal. When a signal with a frequency higher than 20 kHz is being transmitted, it will occupy more than a single channel of bandwidth; as a result, it is necessary to leave adjacent channels empty.

It is also possible for the chip 30 to interface the values from digital sensors by substituting the outputs of the digital sensors for the input signals from the analog-to-digital converter 48. In this manner, at least 13 binary sensors can be sampled every 133 milliseconds. Thus, the interface chip 30 of Fig. 2 is capable of operating in at least four different modes: (1) low frequency analog; (2) high frequency analog; (3) digital data from one or more digital sensors; and, (4) digital data from the external A/D 48.

The ripple counter 32, as illustrated in Figs. 3A and 3B, is driven with a clock signal from the voltage-controlled oscillator 36. The clock signal passes through three buffers 62-66 (Fig. 3A) where the lettering next to each buffer (2X) indicates the sizing of the transistors in the buffer. The ripple counter 32 down-counts the contents thereof where each set/reset flip-flop is clocked by the output from the previous stage. As the counter 32 is down-counted, the output from the last stage flip-flop 82 (Fig. 3B) is applied to the phase/frequency comparator 34. When the content of the counter 32 equals zero, all of the carryout (CO) lines are at a 0 logic level, resulting in the outputs of the NOR gates 84-90, which are part of decoder 38 producing a logic 1 level. When all of the inputs of NAND gate 92 (Fig. 3B) of the decoder 38 are high, set/reset flip-flop 94 produces a load signal at the next clock signal which loads counter flip-flops 68-82 with the frequency selection count supplied from the external chip pins through inverters 130-160 and NAND gates 98-128.

Figure 4 illustrates the details of construction of each of the set/reset flip-flops 68-82 of Fig. 3. A T-switch 170 (transmission switch) supplies a NAND gate 172 with the D input. The gate 172 also receives the reset signal and a signal from switch 174. The switches 170 and 174 are activated with the clock signal. The gate 172 outputs to both switch 178 and gate 176. The set input is connected to gate 176 and gate 182. Gate 182 receives an input from either switch 178 or gate 182. Gate 182 produces an output through buffers 186 and 188 and supplies a signal to gate 184. Gate 184 also receives the reset input.

The output from the counter 32 is applied to the phase/frequency comparator 34 of Fig. 5, along with a reference signal from the timing counter 40. The compared signals are applied to the clock inputs of the set/reset flip-flops 208 and 210 through signal buffers 200-206. When the flip-flops are being clocked at a constant ratio with respect to each other, the NAND 212 resets each flip-flop at the same ratio. When the outputs of the flip-flops are being clocked at the same ratio, the transistors 214 and 216, on the average, produce a constant voltage level at the junction therebetween. Whenever one flip-flop is being clocked at a changing frequency as compared to the other flip-flop, the average voltage produced by transistors 214 and 216 changes. Whenever the counter signal is slowing down, as compared to the reference signal, the output voltage produced by the phase/frequency comparator 34 rises. The rise in the output voltage, after a delay, causes the output voltage produced by the filter 56

to rise, thereby causing the voltage-controlled oscillator 36 to move to a higher frequency. Whenever the ratio is falling, that is, the decoder signal is rising in frequency with respect to the reference signal, the voltage produced by the frequency phase/comparator 34 falls, thereby slowing the voltage-controlled oscillator 36.

The oscillator 42 of Fig. 6 is connected to the oscillator crystal 44 which is off the chip 30 and which can be a TV crystal available from CTI as Model PTI1633. The crystal signal is supplied through buffers 220-228 to the input of the timing counters 40. In addition, the output of the oscillator 42 is supplied external to the chip 30 through a buffer 230 and transistor 232 and 234. The numbers adjacent to transistors 232 and 234 indicate the sizing of the transistors necessary to produce an acceptable output that can be monitored by external circuits.

The timing counters 40 include synchronous D flip-flops 240-268 and asynchronous set D flip-flops to 270-278, as illustrated in Figs. 7A and 7B. The flip-flops have buffers and NAND gates 272-290 connected thereto which provide appropriate signal levels and set the division rate for each stage. The first stage (Fig. 7A), including flip-flops 240-246, is a divide-by-sixteen stage; the second stage, including flip-flops 248-252, is a divide-by-five stage; the third stage, including flip-flops 254-258, is a divide-by-six stage; the fourth stage, including flip-flops 270-278, is a divide-by-thirty-one stage; and the last five stages (Fig. 7B), including flip-flops 260-268, are each divided by two stages. The outputs of the last four stages are applied to NAND gates 292-298 to produce the clock signals for the circuits as indicated. (See also the timing diagram of Fig. 14.) The outputs produced by the NAND gates 292-298, as well as the flip-flops, are buffered by buffers 300-324, so that appropriate signal driving levels can be provided. In addition, the outputs of the high byte enable 294 and low byte enable 292 gates are provided through buffers 326 and 328 and transistors 330-336 to the external pins of the chip 30.

Figure 8 illustrates the construction of the D flip-flops 240-268. The D flip-flops each include a T-switch 340 receiving the D input. The switch 340 supplies buffer 342 which is also supplied by switch 346. The output of buffer 342 is applied to buffer 348 and switch 350. The output of switch 350 is supplied to output switch 354 which is fed back through buffer 356 to switch 352.

Figure 9 illustrates the construction of the asynchronous set D flip-flops 270-278. The asynchronous set D flip-flops each have a construction very similar to the flip-flop of Fig. 8. T-switch 360 receives the D-input and supplies buffer 362 which is also fed by switch 364 via NAND gate 366. The gate 366 receives the set input which is also applied to gate 372. Gate 372 receives another input from switch 368 and produces an output that is fed back through buffer 374 and switch 370.

One of the outputs from the timing counters 40 is provided to the 4 to 1 analog multiplexer 46 illustrated in Fig. 10. The timing signal provided to the multiplexer 46 is oscillating at a frequency of 7.517 Hz, producing windows approximately 133 ms wide, resulting in a complete cycle every 532.1 ms for four conversions. The timing counter signal is applied to D flip-flops 380 and 382 which control NAND gates 384-390. The gates 384-390 produce switching signals which control T-switches 392-398 through buffers 400-414. The multiplexer 46 also provides an address to the shift register 52 which indicates which analog input is currently being output. One bit of the address is produced by exclusive OR gate 416 while the other bit is produced by flip-flop 382. That is, the grey code of the multiplexer is converter to a two-bit binary address output. The address signals are buffered by buffers 418-424 which indicate appropriate sizing. The address supplied to shift register 52 is also supplied as an output of the chip 30 through transistors 426-432. If one of the inputs to the analog multiplexer 46 is connected to ground and/or to a predetermined voltage, the system can provide automatic calibration.

When the A/D converter 48 has converted a single analog input sample, the sample is loaded into the latches 440-464 illustrated in Figs. 11A and 11B one byte at a time. That is, the timing counter 40 provides a low byte enable signal to latches 440-454 which loads the low byte of the sample and a high byte enable signal which subsequently loads the upper five bits of the conversion into latches 456-464. When the latches 456-464 have been loaded, register load signals from the timing counters 40 load the contents of the latches 440-464, as well as the address bits from the multiplexer 46, into dual input D flip-flops 466-500. Once the flip-flops 466-500 are loaded, a clock signal, at a frequency of 120.28 Hz, from the timing counters 40 clocks the contents of the flip-flops 466-500 serially to the Manchester encoder 54.

The details of construction of each of the single bit latches 440-464 of Fig. 11 are illustrated in Fig. 12. Each single bit latch includes a T-switch 510 receiving the input and supplying same to a buffer 514. The output of buffer 514 is fed back through buffer 516 and switch 512.

The details of construction of each of the dual input D flip-flops 466-500 of Fig. 11 are illustrated in Fig. 13. The dual input flip-flops receive one input through a T-switch 520 and the other input through switch 522. Both switches 520 and 522 supply switch 524. The output of switch 524 is applied to switch 528 and fed back through buffer 530 and switch 526. The outputs are produced by switch 532 through buffers 536 and 538. Switch 534 feeds back the inverted output.

The timing associated with the sampling by the analog-to-digital converter 48, loading of the sample into the latches 440-464, transfer from the latches 440-464 to the shift register flip-flops 466-500, and the clocking of the samples serially to the encoder 54 is illustrated in Fig. 14. The top waveform indicates the clocking of the bits from the shift register 52 into the encoder 54 where the number within the waveform indicates the particular data bit being clocked. After the high byte and low bytes have been enabled (Fig. 14A), the digital-to-analog

converter 48 begins an integration period followed by a deintegration period (Fig. 14B). During the deintegration period, the shift register 52 is loaded with the previous sample stored by the latch 50. This load enable corresponds to a dead period in the serial transmission of the shift register bits to the encoder 54. Near the end of the deintegration period, a valid data period starts during which the high and low bytes from the converter 48 are stored in the latch 50. Before a new integration cycle occurs, a delay is seen at the A/D converter 48 when using the RUN/HOLD as the clock. The delay period is approximately 113 microseconds after the low byte is latched and the multiplexer 46 is clocked.

The serial bits from the shift register 52 are applied to an exclusive OR gate 550 in the Manchester encoder 54, illustrated in Fig. 15. The other input of the gate 550 receives a 120 hertz timing signal from timing counters 40. the output of gate 550 is applied to a D flip-flop 552, the construction of which is illustrated in Fig. 8. The clock signals for D flip-flop 552 and D flip-flop 554 are supplied from the timing counters 40 through buffers 556 and 558 at 240 Hz. The output of flip-flop 552 is applied to an output line through buffers 560 and 562 and T-switch 564. The output of flip-flop 554 is applied through buffers 566 and 568 controls the switch 570 is applied to and one control input of T-switch 564.

Figure 16 illustrates the timing diagram for the Manchester encoder 54. As can be seen from the timing diagram, the Manchester encoder 54 produces a signal that is on the average, zero volts. Such a signal is very important when a carrier frequency is being modulated and controlled by a voltage-controlled oscillator. The use of the Manchester encoder 54 ensures that, on the average, the encoded signal produces the carrier frequency.

Figure 17 illustrates the loop filter amplifier 58 where, once again, the sizing of the transistors 580 and 582 is illustrated by the sizing numbers adjacent thereto.

The filter 56 can be ordinary 3 pole, or if higher accuracy is required, a 5-pole filter which will produce a time constant of approximately 40 seconds allowing the voltage-controlled oscillator 36 to receive a very steady input signal. One of ordinary skill in the art can provide an appropriate filter by reviewing a filters designs book on phase-locked loops such as the Phase Locked Loop chapter of the Motorola MECL Data Book, 1982.

The voltage-controlled oscillator 36 is a standard ring-type oscillator, as illustrated in Fig. 18. The ring-type oscillator consists of cascade-connected P (592 and 594) and N (590) transistors producing eleven inverter stages where the output of the transistor in the final stage is connected back to drive the input of the first stage. The output of the ring oscillator is buffered by buffers 596-602 to increase its signal level before being applied to the transformer 60 of the coaxial cable 4. The buffers, once again, indicate transistor sizing. An auxiliary output is provided through buffer 604 which is connected to an external pin of chip 30 for connection to the ripple counter 32. the voltage-controlled oscillator 36 produces greater than 60 dB signal-to-noise. Each channel is 44.7 kHz wide, allowing 128 channels within one octave and thereby eliminating harmonic distortion considerations. The voltage-controlled oscillator 36 is not hard-wired back to the ripple counter 32 so that an external voltage-controlled oscillator can be used, if desired.

To allow the present invention to interface conveniently with other devices which use zero to five volts while still maintaining plus five to minus five-volt logic within the chip, level shift circuits are provided between each input pin and the internal chip circuits and between the internal chip circuit and each output pin. An example of a level shift circuit is illustrated in Fig. 19 where, once again, the appropriate transistor sizings are indicated. Each level shift circuit includes transistors 610-624 and buffer 626.

Figures 20 and 21, including 21A and 21B, illustrate the mask and layout, respectively, of the integrated circuit analog serial bus interface chip 30, where Fig. 20 illustrates the mask layout and Fig. 21 illustrates the relationship between the various circuits and between the circuits and the exterior chip connections. As can be seen in Figs. 21A and 21B, the ripple counter 32 is located (Fig. 21A) in the upper left-hand corner associated with side IV and with the phase locked loop bonding tabs which set the frequency of the frequency synthesizer. Below the ripple counter 32 is the decoder 38 (Fig. 21B) followed by the phase/frequency comparator 34. The voltage-controlled oscillator 36 is generally located in the lower left-hand corner and is surrounded by power supply lines, as illustrated in Fig. 20, so that the analog output signal produced by the voltage-controlled oscillator 36 will be relatively free of the noise generated by the digital circuitry on the chip. This physical isolation is also provided to loop filter 58 which is below the voltage-controlled oscillator 36. The voltage-controlled oscillator 36 and amplifier 58 are powered by analog power supply bonding tabs located along the bottom side (side III) of the chip while the digital circuitry has its own power supply tabs located on sides II and IV. The separation of the power supply bonding tabs reduces noise coupled to the network.

In the center of the chip, running vertically, are the timing counters 40. The timing counters 40 are located centrally because they must provide timing signals throughout the chip. The central location minimizes the length of high and low frequency signal runs within the chip. In the center of the timing counters 52 is a 10 kHz line running from one count stage at the bottom to a count stage at the top. The 10 kHz signal line is shielded on both sides by power supply lines. The oscillator 42 driving the chip is located above the timing counters 40.

The latch 50 is located between the folded shift registers 52 so that each shift register will receive its data from the closest latch. The two bits of the shift register 52 which receive the address from the analog multiplexer 46 (Fig. 21B) are located adjacent to the multiplexer 46. The output of the shift register 52 is buffered through buffers 630 and coupled to the Manchester encoder 54 located next to the end of the register 52 where the serial bits emerge. The analog multiplexer 46 is located in the bottom right

corner of the chip. The location in the corner allows the inputs to enter and the output to exit the chip without the need for signal crossover lines; this arrangement reduces noise coupled from the chip 30. ON the right side of the chip are level shift circuits 632 which match the input signals from the analog-to-digital converter 48 with the signal level of the chip 30.

As can be seen from the pin layout in Figs. 21A and 21B, all digital signals are generally on the upper half of the chip while all analog signals are on the lower half of the chip. This arrangement, once again, isolates noise sensitive analog signal lines from the noise creating digital signal input lines. The high frequency inputs for the oscillator crystal 44 are located at the top (side I) as far from the channel signal (output #2, side III) produced by the voltage-controlled oscillator 31. The lead tabs each have notches which divide each tab into two portions. Each portion is large enough to accept a lead, so that if a bonding error occurs the bonder can try again. The chip is oriented in its chip carrier with sides I and III toward the narrow side of the carrier to minimize the length of the analog signal lines, thereby increasing noise immunity.

The chip 30 is created using a standard CMOS process, the details of which are available from a plurality of sources, including:

Modern MOS Technology
Dewitt G. Ong, McGraw Hill, 1984.

The Physics of Semiconductor Devices
D. M. Sze, Wiley & Sons, 1984.

Microelectronics-Processing & Device Design
Roy A. Colclaser, Wiley & Sons, 1980.

VLSI Technology
S. M. Sze, McGraw-Hill, 1983.

Integrated Circuit Fabrication Technology
David J. Elliot, McGraw-Hill, 1982.

One of ordinary skill in the art can create a chip with a layout, as illustrated in Fig. 21 from the teachings of the above-listed books incorporated by reference herein.

As mentioned previously with respect to Fig. 1, the coaxial cable 4 is typically supplied with 60-cycle, 28-volt alternating current from a power supply in buffer 2, as illustrated in Fig. 22. A transformer 640 converts the 120-volt, 60-cycle signal into the signal which is coupled to the coaxial cable 4 through inductors 642 and 644 of 51 pico henrys each. The returning frequency division multiplexed signal from the remote units 6 is coupled through a capacitor 646 and an ordinary radio frequency transformer 648. The signal is then passed through a six to twelve megahertz bandpass filter 650 after which is it amplified by an amplifier unit 652 which comprises series coupled HA-2540 and HA-5002 amplifiers available from Harris. The buffer board also includes a crystal oscillator 654 which is tuned to a reference of 3.579 MHz and a divide-by-10 circuit which divides the reference frequency by a factor of 10.

Each receiver 6, as illustrated in Fig. 22, includes a microcomputer 660 which controls a frequency synthesizer 662 to synthesize the carrier frequency of the remote unit to which the receiver corresponds. The frequency synthesizer 662 includes a programmable frequency divider which converts the crystal oscillator signal to the appropriate carrier frequency. The frequency synthesizer 662 includes a frequency synthesizer Model MC145156 from Motorola, a divider Model MC3393 from Motorola and voltage-controlled oscillator Model C1648 from Motorola and a filter which is a 40 megahertz standard design lowpass filter designed to remove high frequency noise from the synthesized carrier signal. The synthesized carrier signal is mixed in mixer 664, such as an SL6440 From Plessey, with the modulated carriers for the various receivers provided by amplifier 652. The mixed signal is provided to a crystal filter 666 operating at a frequency of 21.4 megahertz. The crystal filter 666 selects only the channel of interest and attenuates all others. The output from the crystal filter 666 is applied to an FM detector 668 such as a CA3089 available from RCA. The FM detector demodulates and removes the carrier leaving either. the Manchester encoded signal or the high/low frequency analog signal transmitted by the respective remote unit 6.

If an analog signal is being transmitted by the remote unit 6, the demodulated signal is passed through a programmable attenuator 670, made with a resistor network and an analog multiplexer, such as an MC14052. The gain controlled analog signal is then applied to an amplifier 672, such as an LM 386-4 available from National Semiconductor, before the signal is output. If the Manchester encoded signal is the signal transmitted by the corresponding remote unit 6, comparators 674, such as an LM139 available from National Semiconductor, are used to determine the state of the transmitted signal and provide same to microcomputer 660. The microcomputer is preferably an 8731, available from Intel with appropriate ROM memory for storing a control program.

Figure 23 illustrates conceptually the operation of the microcomputer 660 of Fig. 22. The routine of Fig. 23 monitors a communication link to the computer 14 for commands therefrom and is interrupted by an interrupt timer to perform detection of encoded bits transmitted to the receiver 12 from the associated remote unit 6. The interrupt routine is discussed, in general, with respect to Fig. 27 and, in more detail, with respect to Fig. 28. After a power-on reset occurs 700 and the microcomputer 660 is initialized 702, the microcomputer 660 retrieves 704 the receiver frequency from the bus to computer 14 and loads 706 the frequency synthesizer 662 with the appropriate frequency designation word. Next, the processor 660 sets 708 the interrupt timer to 200 microseconds. That is, at the end of 200 microseconds the processor will examine the comparators 674 to determine whether a start bit has been received from the Manchester encoder 54 of the respective remote unit 6. The microcomputer 660 then enters into a loop wherein the bus from computer 14 is periodically examined to determine if a command has been received from the computer 14. The commands include tasks

associated with updating 712 the synthesizer frequency, sending 714 the last encoded word, sending 716 the last four encoded words, sending 718 the last sixteen encoded words, sending 720 the current frequency and sending 722 a self-test.

At the beginning of the control routine, as illustrated in Fig. 24A during the power on reset function, the address for the input from the computer 14 bus is stored 730, after which the count register (TCON), interrupt enable register (IE), interrupt priority register (IP), serial count register (SCON) and program status word register (PSW) are initialized 732. Next, the microcomputer 660 begins monitoring the bus to computer 14 to determine whether a frequency word for this particular microcomputer (receiver) has been received. The first step is to examine 734 the receive interrupt flag to determine whether it has been set, indicating that the frequency word has been received. If the receive/interrupt flag has been set, then the microcomputer 660 examines 736 the most significant bit to determine whether it is a 1. If it is not a 1, the receive interrupt flag is set 738 to 0 and the microcomputer 660 continues examining words. If the most significant bit is a 1, then the microcomputer determines 740 whether the word is addressed to itself and then determines 742 whether the word is a frequency designation word. If it is a frequency designation word, the receive interrupt flag is set 744 to 0 followed by a check 746 to determine whether there has been another receive interrupt. If an interrupt has not occurred, then the most significant bit of a valid frequency (0-127) must always be zero. This serves as an additional check to make sure that the data is valid before the synthesizer is loaded. Once the microcomputer 660 has determined that the received word is the frequency designation word, the frequency is stored in the buffer for the frequency synthesizer. P3.5 and P3.6 (Fig. 24B) are microcomputer 660 output lines used to load data serially into the synthesizer 662. Next, the synthesizer update routine is called 752. This routine loads the designated frequency into the frequency synthesizer 662 and will be discussed in more detail with respect to Fig. 25. Once the frequency has been set, various flags and counters are set 754, after which the interrupt timer is set 756 to 200 microseconds. Next, the interrupt enable flag is set and the timer count register is started 758.

The loop depicted in Fig. 23 is illustrated in more detail in Figs. 24C and 24F. The program enters into a loop during which the receive interrupt flag is checked 760 (Fig. 24C) to determine whether a word has been received. If a word has been received, the interrupt flag is set 762 to 0 zero followed by a determination 764 as to whether the word is addressed to this receiver. If the word is addressed to this receiver, a check 766 is made to determine whether the most significant bit is 1. If the most significant bit is 1, the flag which indicates that a communication has been received is set 768 to 0. Next, a check 770 is made to determine whether the word is a frequency update command; and if so, the receiver enters a loop in which the receive interrupt flag is checked 772 until a word has been received. The receive interrupt flag is then set 774 to 0, after which the most significant bit is examined 776 (Fig. 24D) to determine whether it is 0. If so, it indicates that a correct frequency specification word has been received and the frequency is loaded 778 into the frequency synthesizer variable. The interrupt timer is then disabled 780 and the counter is disabled 782. Next, the synthesizer update subroutine is called 784 to update the frequency produced by the synthesizer 662. After the frequency update, the appropriate pointers and flags are updated 786 followed by the setting 788 of the interrupt timer to 200 microseconds. Once the interrupt timer has been set, the timer is enabled 790 and the timer count register is also enabled 792.

If the word received was not a frequency update word, then the processor determines 794 (Fig. 24E) whether a valid request has been received and, if so, executes the appropriate function. If an invalid request has been received 796, the bad word is just ignored.

If a command for sending words is detected, an array counter is set 798-802 to the appropriate value. The starting address (X) of the word of words to be transmitted is then stored 802 and the process enters a loop (Fig. 24F) during which the word of words are transmitted. During this loop, the send subroutine is called 812 and will be discussed in more detail with respect to Fig. 26.

If one of the other commands has been detected, the appropriate word is loaded 816 (Fig. 24F) and 818 into the transmit buffer or the appropriate self-test flag is set 820 to 0. If the transmission of the frequency or self-test is required, the program status word bit for enabling the bus is set 822 to 0 after which the call subroutine is executed 824. When the last word has been transmitted, the transmit interrupt flag will be set to 1 and the receiving communication flag will be set 828 to 1. Next, the program status word bit is updated 830 to set the bus connection between the microcomputer 660 and the common bus to a high impedance state. The bus connection between the computer 34 and microcomputer 660 is a tristate bus in which the bus connection can be set to a high impedance state whenever the microcomputer 660 is not accessing the bus.

Figure 25 illustrates the details of the subroutine which loads the frequency synthesizer 662 with the appropriate frequency designation word. First, the gain bits for the synthesizer are set 842 followed by the setting 844 of the indicated bits. P3.7 is the data output and P3.6 is the frequency synthesizer 66Z clock. Step 844 clocks a 0 into the most significant bit of the synthesizer 662. Next, the bit pattern for the designated output frequency is retrieved 846 from a look-up table which includes 128 words where each word corresponds to the frequency of a possible channel to be received by the receiver 6. The look-up table, which correlates frequency or channel number with synthesizer bit pattern, can be created by one of ordinary skill in the art. Next, the microcomputer 660 enters a loop. During this loop using P3.7 as the output port and P3.6 as the clock, the loop shifts 858 the data to the left and by

comparing 850 the word to 32767, determines if the next data bit to the synthesizer should be a 1 or 0. That is, if the word is greater than the constant, the output bit is set 854 to 1; otherwise, it is set 851 to 0. When the appropriate frequency is loaded, the microcomputer 660 latches 862 the new frequency by toggling the appropriate bit of the program status word. The processor then waits 80 milliseconds to allow the synthesizer to switch to the new frequency before returning 866.

Figure 26 depicts the details of the send subroutine in which the transmit interrupt flag is checked 872 to determine whether it is a 1 indicating that the bus is not occupied. If the bus is not occupied, the transmit interrupt flag is set to 0, indicating that the bus is occupied and the contents of the buffer are loaded into the transmitter. The contents of the variable XMIT is loaded into a buffer named SBUF and the buffer proceeds to shift out the word. Once the contents of the buffer are transmitted, the routine returns 878.

The interrupt routine, illustrated conceptually in Figs. 27A and 27B, begins by determining 892 (Fig. 27B) whether the start bit flag is set. If the flag is set, a determination is made 894 (Fig. 27A) concerning whether the bit being detected is the start bit. The start bit is detected by one of the comparators 674 outputting a signal indicating the input signal is high and the other of the comparators indicating that the input signal is low. That is, the start signal is between the high and low values, as depicted in Fig. 16A. If the start bit is being detected, the width counter is incremented 896 followed by the setting 898 of the interrupt timer to 200 microseconds, an interval that allows an accurate determination of the width and end of the start bit. That is, while the start bit is being detected, the width of the start bit is being measured by the interrupts. If the start bit is not being detected, determination is made 900 as to whether the start bit has a zero width. If so, the interrupt timer is set 898 to 200 microseconds and the microcomputer will continue to look for a start bit of non-zero width. If the start bit has a non-zero width, a determination is made 902 whether the start bit is of the correct width. If the correct width has not yet been detected, the the timer is once against set to 200 microseconds and another interrupt is awaited. If the start bit is of the correct width, the start bit flag is reset 904 and the timer between interrupts is set 906 to a longer period of 2.6 milliseconds. The 2.6 millisecond interval should cause an interrupt in the middle of the first data bit. A start bit is preferably 8.31 milliseconds wide and each data bit is 8.31 milliseconds wide.

If the start bit flag is not set and an interrupt has occurred, the microcomputer shifts 908 (Fig. 27B) in the data bit. The value of a data bit can be determined by examining the output produced by only one of the comparators. The microcomputer 660 then determines 910 whether this is the last bit of the word, and if not, sets the interrupt timer to the interval between data bits (8.31 milliseconds). If the bit is the last bit of the word, then the word is stored 914 and the start bit flag is set 916, followed by the setting of the timer for the deadband interval between the end of the last bit and the beginning of the start bit of the next encoded word.

Figs. 28A and 28B illustrate the interrupt routine of Fig. 27 in greater detail whereby the flags, status bits, etc., are examined. First, the register bank pointer to the bank, which is used for storing the incoming word, is set 930 (Fig. 28A) to 1, followed by disabling 932 of the timer counter register. Then the start bit flag, as previously discussed, is examined 934, followed by a comparison 936 of the indicated input bits. These bits indicate whether a start bit level is detected. If the start bit counter value is greater than 39, the value of the self-test word is examined 940 (Fig. 28C). If the value of the self-test word is not 7F, the self-test counter is incremented by one, followed by a setting 946 of the start bit counter to 0. A value of 7F indicates 128 start bits have not been detected. The bit counter indicates which bit of an encoded word is presently being input. When the start bit counter is less than 39, it is examined 948 to determined whether the start bit counter is greater than or equal to 24. If not, the start bit counter is examined 950; and if it is 0, another self-test check is performed; otherwise, the start bit counter is set 946 to 0. If the start bit counter is greater than or equal to 24, the program status bit indicated is set 952 to 1, followed by the setting 954-958 of various flags and values to 0. The interrupt timer is also set 960, followed by setting the program status word bit indicated to zero. If the start bit has been detected, the start bit counter is examined 962 (Fig. 28A) to determine whether it is at its maximum value. If not, the start bit counter is incremented 964, followed by the setting 966 (Fig. 28B) of the interrupt timer at the value for continuing to examine the start bit.

If the start bit flag is not equal to 1, the program status bit for setting the strobe high is set 968 (Fig. 28A) to 0. Next, the data word is shifted 970 left, by one, followed by a check 972 of the input data bit indicated to determined whether the incoming bit is a 1 or a 0. If the incoming bit is equal to 1, a 1 is added 974 (Fig. 28B) to the data word. If the incoming bit status word bit is equal to 0, a 0 is added 976 to the data word. Block 976 is intended to equalize the program delay associated with adding in block 974.

Next, the bit counter is incremented 978, followed by setting 980 the test point I/O bit indicated to 0. If the bit counter is determined 982 to be equal to 15, then the end of the word has been detected and the array pointer for storing the word is updated 984. If the array pointer is equal to 17, then the last word in the array available for storing incoming data has been filled and the pointer must rotate back to the beginning of the array by setting 988 the array pointer back to 0. Once a valid array pointer has been determined, the data is stored 990 in the appropriate location of the incoming buffer. The interrupt timer is then set 992 to 4.1 milliseconds to detect the next incoming data bit. If the bit counter is not equal to 15, then the interrupt timer is set 994 to a value appropriate for detecting the next data bit. Once the interrupt timer has been set to the proper value, the counter is enabled 996, followed by the

setting 998 of the register bank to 0.

The many features and advantages of the invention are apparent from the detailed specification, and thus it is intended by the appended claims to cover all such features and advantages of the invention which fall within the true spirit and scope thereof. Further, since numerous modifications and changes will readily occur to those skilled in the art, it is not desired to limit the invention to the exact construction and operation illustrated and described; and, accordingly, all suitable modifications and equivalents may be resorted to, falling within the scope of the invention.

Claims

1. A common bus multinode sensor system for at least one sensor (8/10 or 22/24) to convey a sensor signal, comprising

a power supply (640);

a communication cable (4), coupled to and carrying said power supply;

remote sensor means (6), coupled between said cable (4), and said sensor, characterized by:

means providing a carrier and for frequency-division multiplexing the sensor signal onto said cable and receiving power from said cable; and

receiver means (12), coupled to said cable, for demultiplexing the frequency division multiplexed sensor signal.

2. A system as recited in claim 1, wherein said remote sensor means (6) comprises:

programmable carrier frequency means (32-42) for providing a carrier to said cable at a carrier frequency in dependence on an external input; and

modulation means (56) for frequency modulating the carrier with the sensor signal.

3. A system as recited in claim 2, wherein said carrier frequency means comprises:

reference frequency means for providing a reference frequency;

a counter (32) counting in accordance with the external input and providing a divided count frequency;

a phase/frequency comparator (34), operatively connected to said counter and said reference frequency means (42), for comparing the divided count frequency to the reference frequency and providing a voltage indicative of the comparison; and

a voltage-controlled oscillator (36), operatively connected to said phase/frequency comparator (34) and said cable (4), producing the carrier at a frequency dependent on the voltage.

4. A system as recited in claim 3, wherein said modulation means (56) comprises a filter, operatively connected to said phase/frequency comparator (34), the sensor and said voltage-controlled oscillator, for averaging the voltage produced by said phase/frequency comparator and for combining the averaged voltage with the sensor signal and providing the combination to said voltage-controlled oscillator (36).

5. A sensor system as recited in claim 2, coupled to several sensors producing several sensor signals and said remote sensor means further comprises multiplexing means for time division multiplexing the sensor signals.

6. A system as recited in claim 5, wherein said remote sensor means further comprises encoding means (48, 54) for encoding the multiplexed sensor signals.

7. A system as recited in claim 6, wherein said encoding means comprises:

an analog-to-digital converter (48) operatively connected to said multiplexing means and converting the analog signals into digital data; and

an encoder operatively connected to said analog-to-digital converter and said modulation means, and encoding the digital data and applying the data to said modulating means for modulating the carrier.

8. A system as recited in claim 1, wherein said receiver means (12) comprises:

synthesis means (662) for producing a mixing frequency; and

mixing and detection means (644, 666, 668) for combining the frequency division multiplexed sensor signal and the mixing frequency, and producing a frequency division demultiplexed signal.

9. A system as recited in claim 1, wherein said remote sensor means encodes the sensor signal, and said receiver means includes decoder means for decoding the encoded sensor signal.

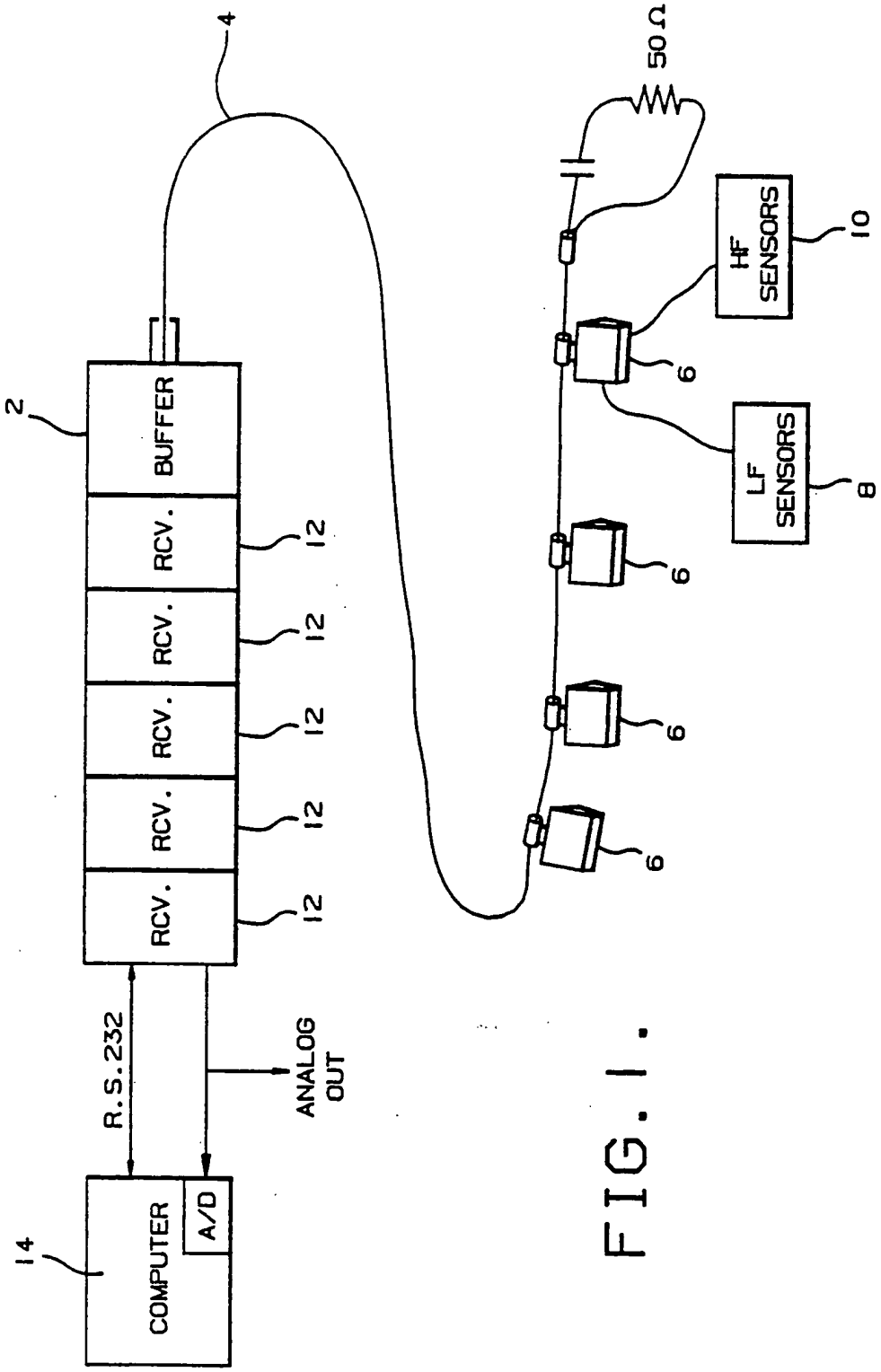

4
50 Ω
HF SENSORS
10
6
LF SENSORS
8
6
6
6
2
BUFFER
RCV.
12
RCV.
12
RCV.
12
RCV.
12
RCV.
12
R.S.232
ANALOG OUT
14
COMPUTER
A/D

FIG. 1.

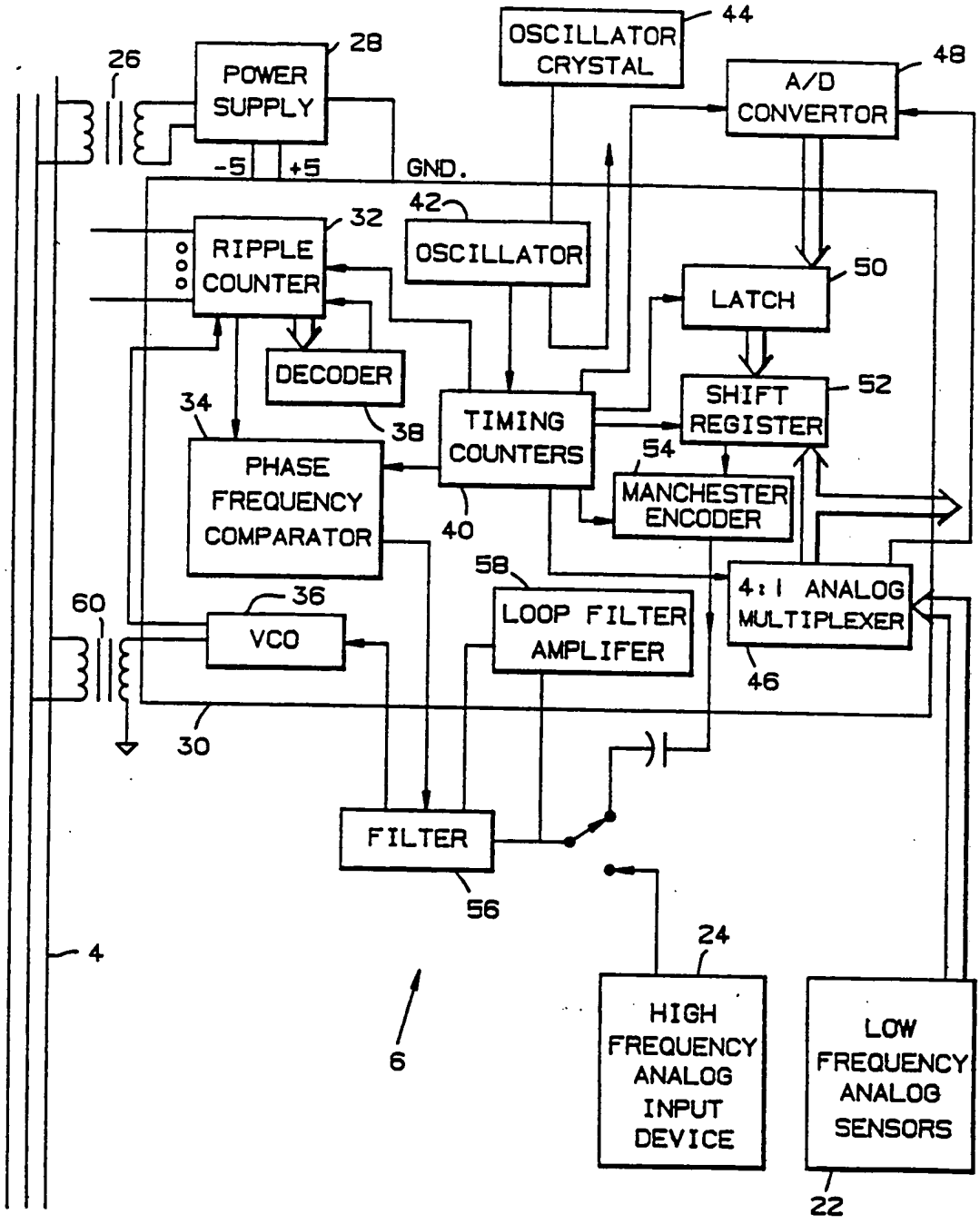

OSCILLATOR CRYSTAL
44
A/D CONVERTOR
48
26
POWER SUPPLY
28
-5
+5
GND.
42
OSCILLATOR
32
RIPPLE COUNTER
LATCH
50
DECODER
38
SHIFT REGISTER
52
34
TIMING COUNTERS
54
PHASE FREQUENCY COMPARATOR
40
MANCHESTER ENCODER
58
4:1 ANALOG MULTIPLEXER
60
36
VCO
LOOP FILTER AMPLIFER
46
30
FILTER
56
4
24
6
HIGH FREQUENCY ANALOG INPUT DEVICE
LOW FREQUENCY ANALOG SENSORS
22

FIG. 2.

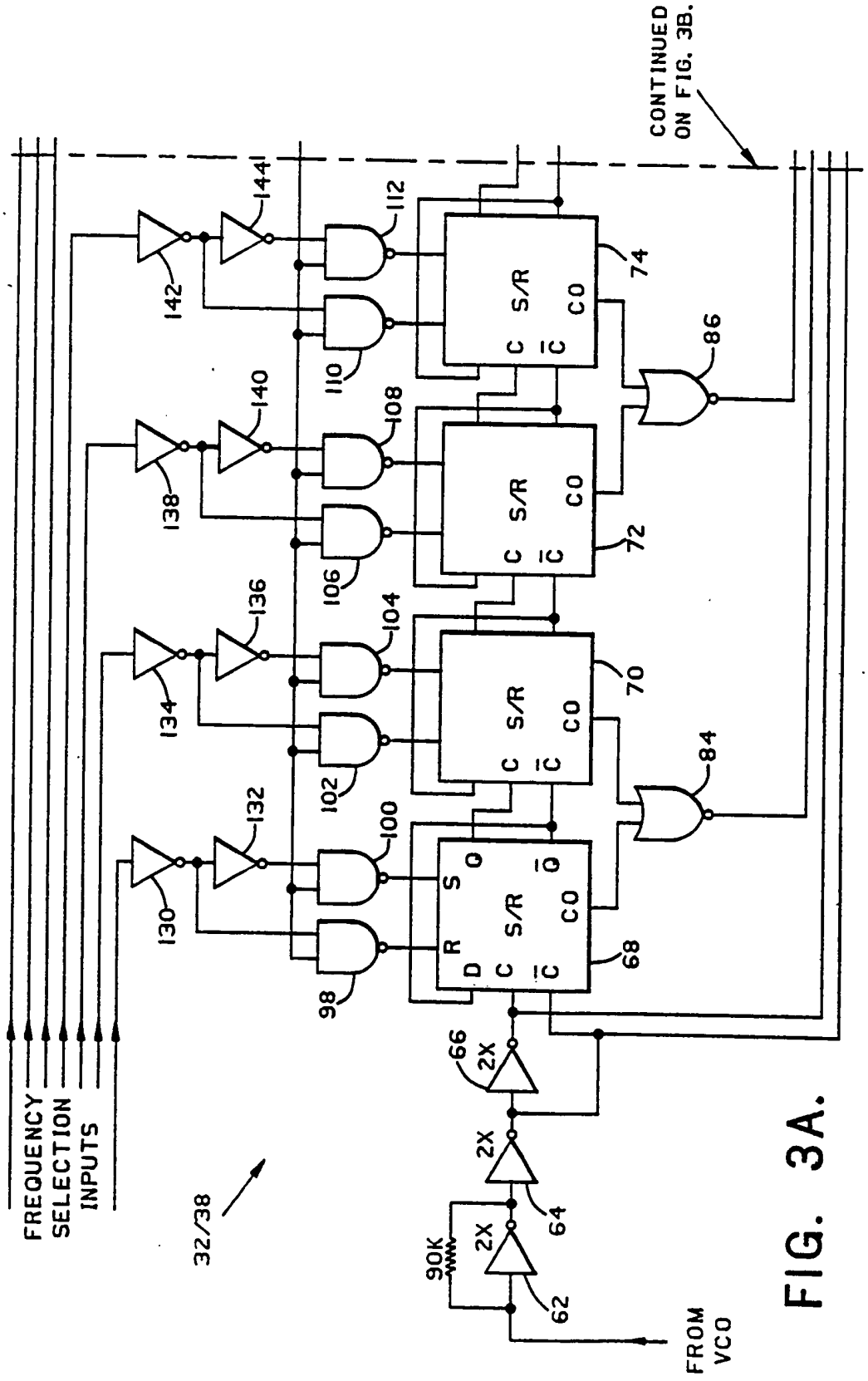
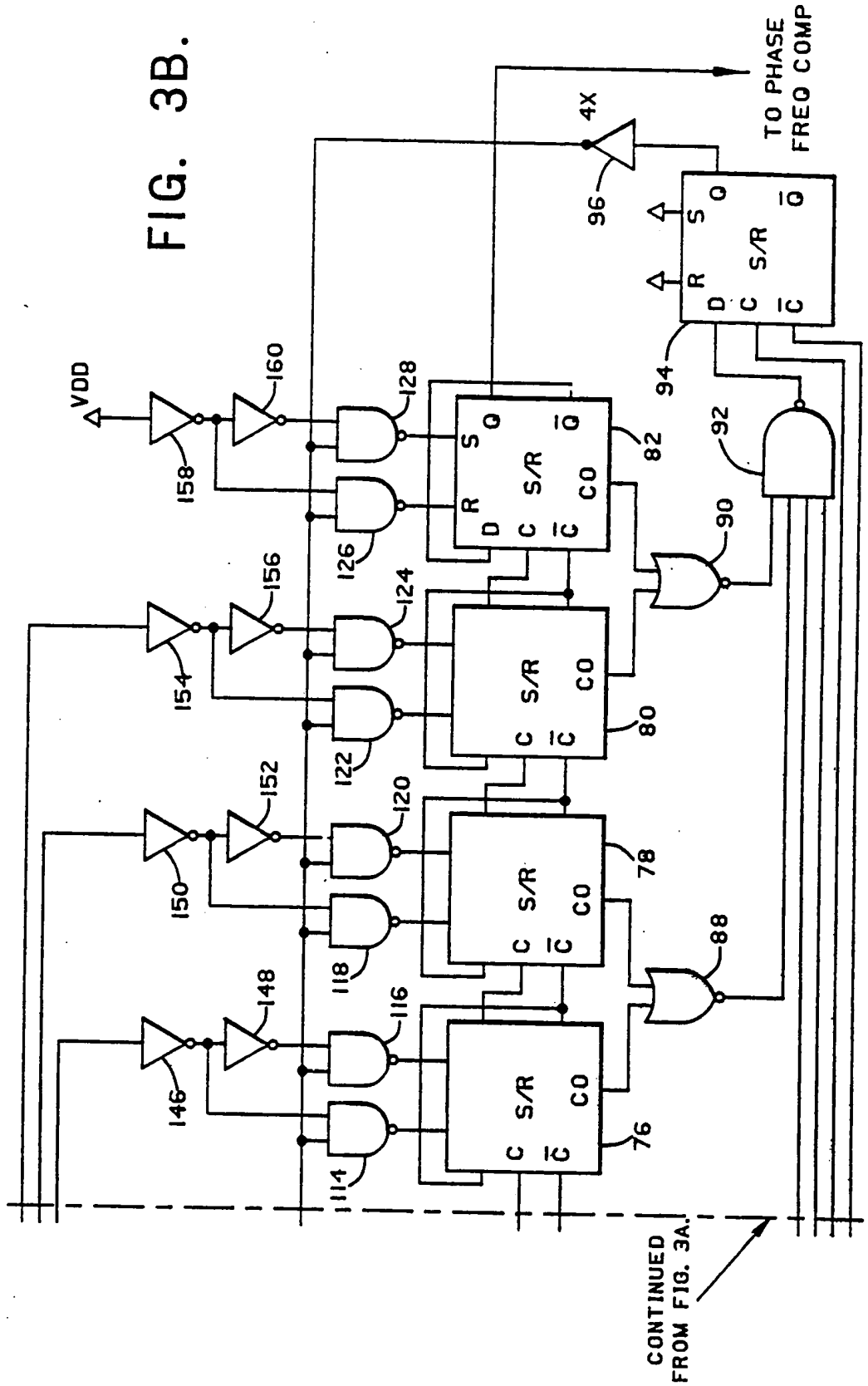

CONTINUED ON FIG. 3B.
FREQUENCY SELECTION INPUTS
32/38
FROM VCO
90K
2X
64
66
62
68
70
72
74
84
86
98
100
102
104
106
108
110
112
130
132
134
136
138
140
142
144
S/R
CO
C
S
R
D
Q

FIG. 3A.

FIG. 3B.


TO PHASE FREQ COMP
4X
96
94
92
90
88
82
80
78
76
VDD
158
160
154
156
150
152
146
148
128
126
124
122
120
118
116
114
S/R
CONTINUED FROM FIG. 3A.

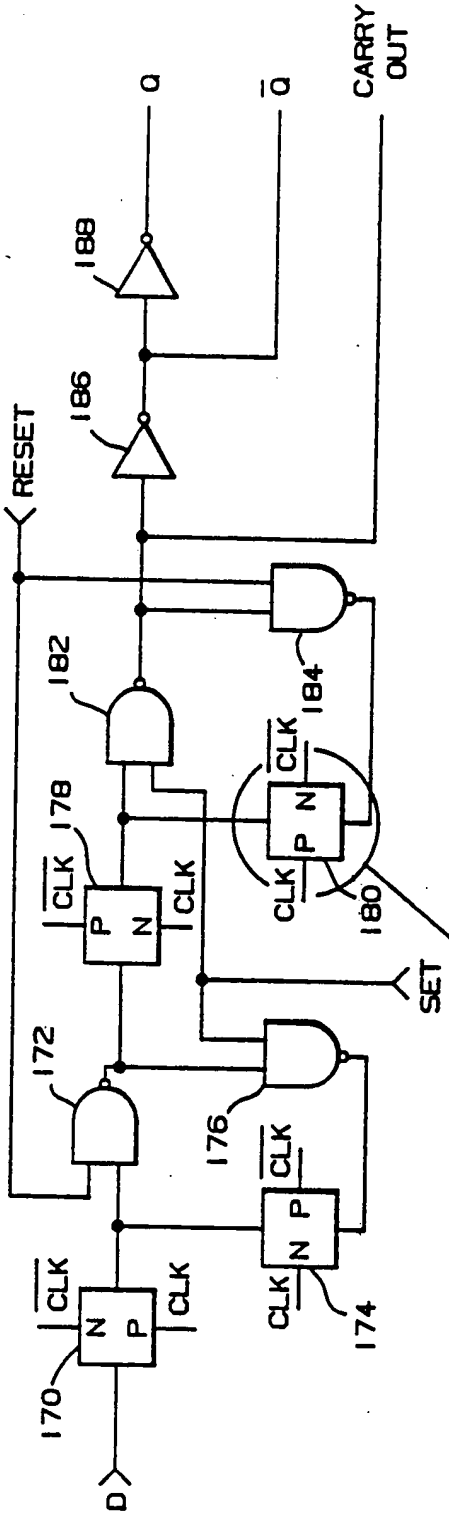

Q
$\bar{Q}$
CARRY OUT
188
186
RESET
182
184
178
CLK
P
N
180
SET
172
176
174
170
D

FIG. 4.

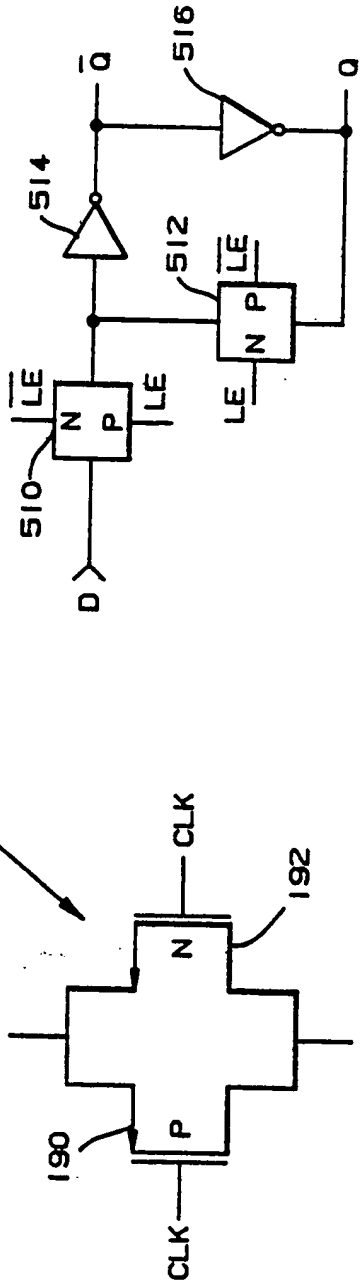

$\bar{Q}$
516
Q
514
512
LE
510
D
CLK
192
190

FIG. 12.

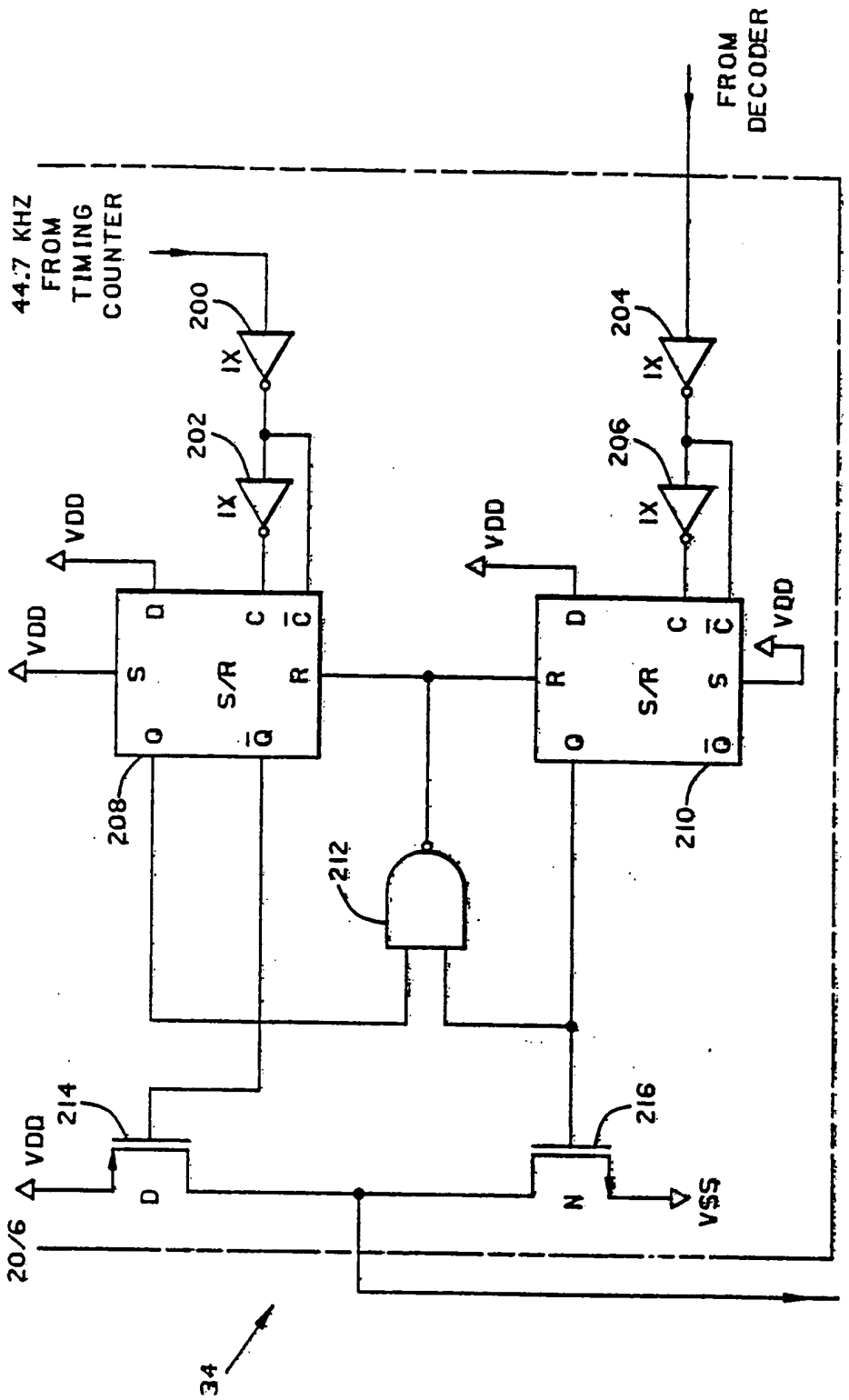

FROM DECODER
44.7 KHZ FROM TIMING COUNTER
200
202
204
206
1X
VDD
S/R
D
C
S
R
Q
208
210
212
214
216
VSS
20/6
34
TO FILTER

FIG. 5.

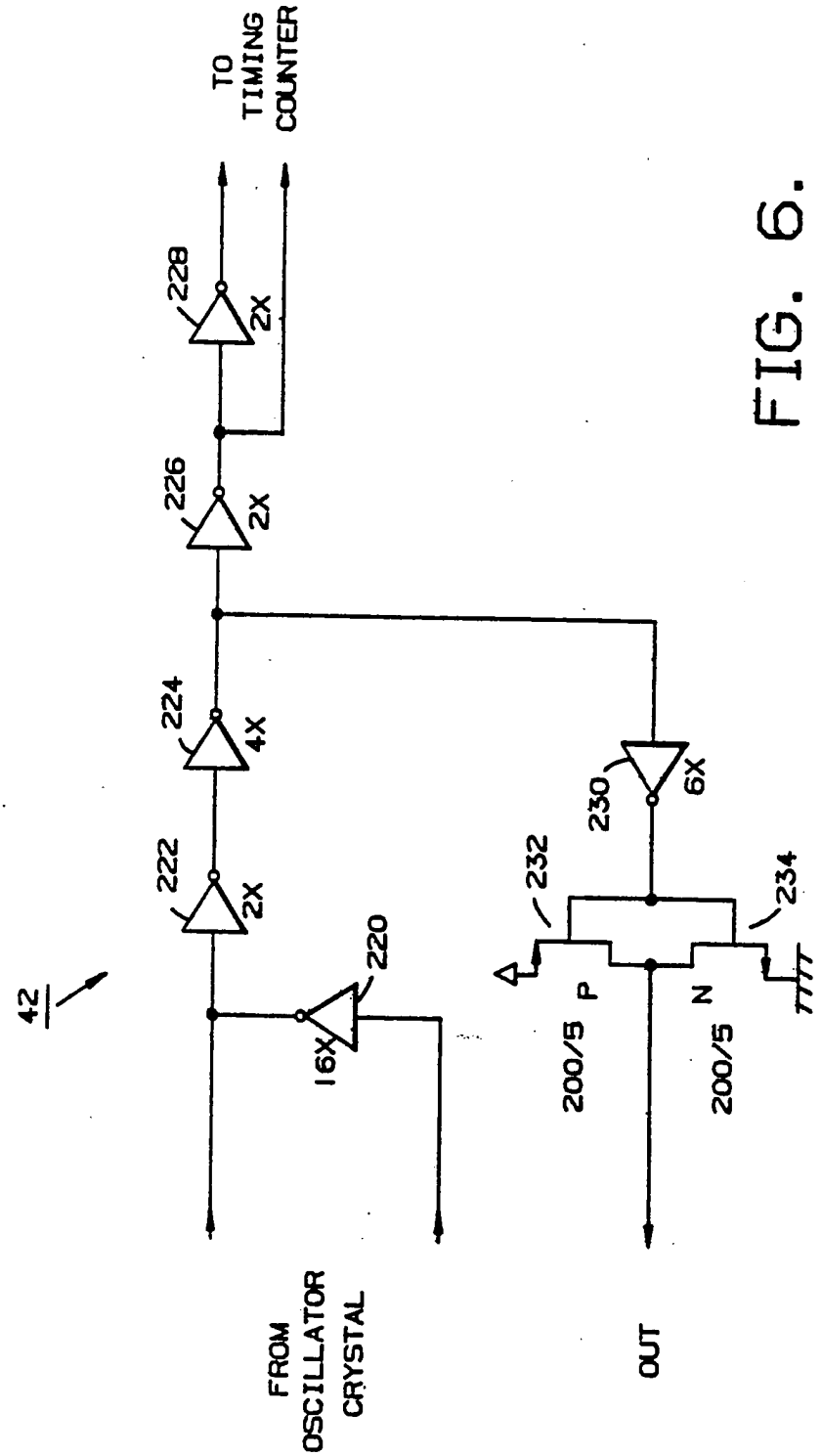

42
FROM OSCILLATOR CRYSTAL
220
16X
222
2X
224
4X
226
2X
228
2X
TO TIMING COUNTER
230
6X
232
200/5 P
234
200/5 N
OUT

FIG. 6.

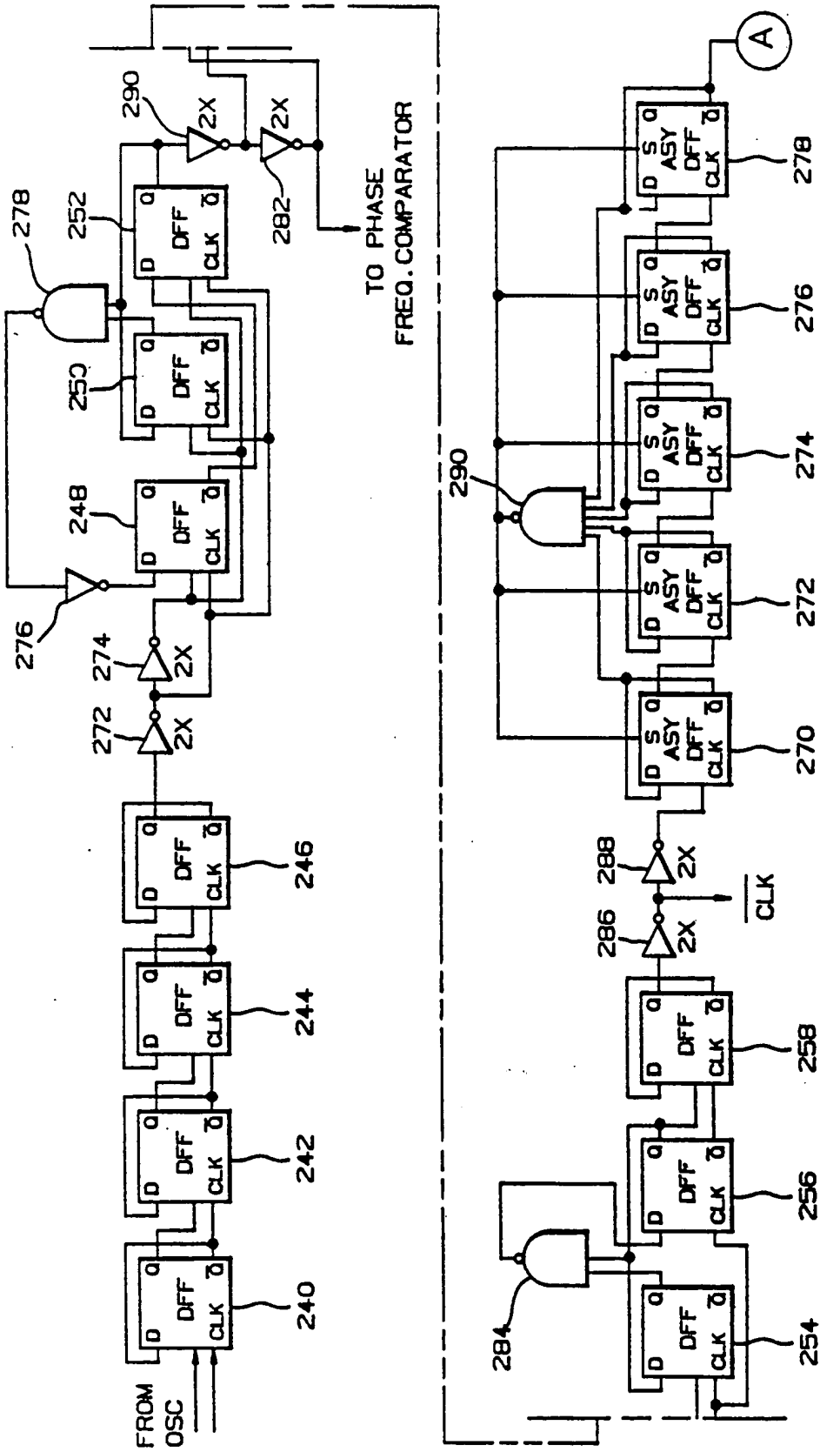

FROM OSC
240
242
244
246
DFF
CLK
D
Q
248
250
252
278
276
274
272
2X
290
282
TO PHASE FREQ. COMPARATOR
A
ASY DFF
S
270
272
274
276
278
288
286
CLK
258
256
254
284

FIG. 7A.

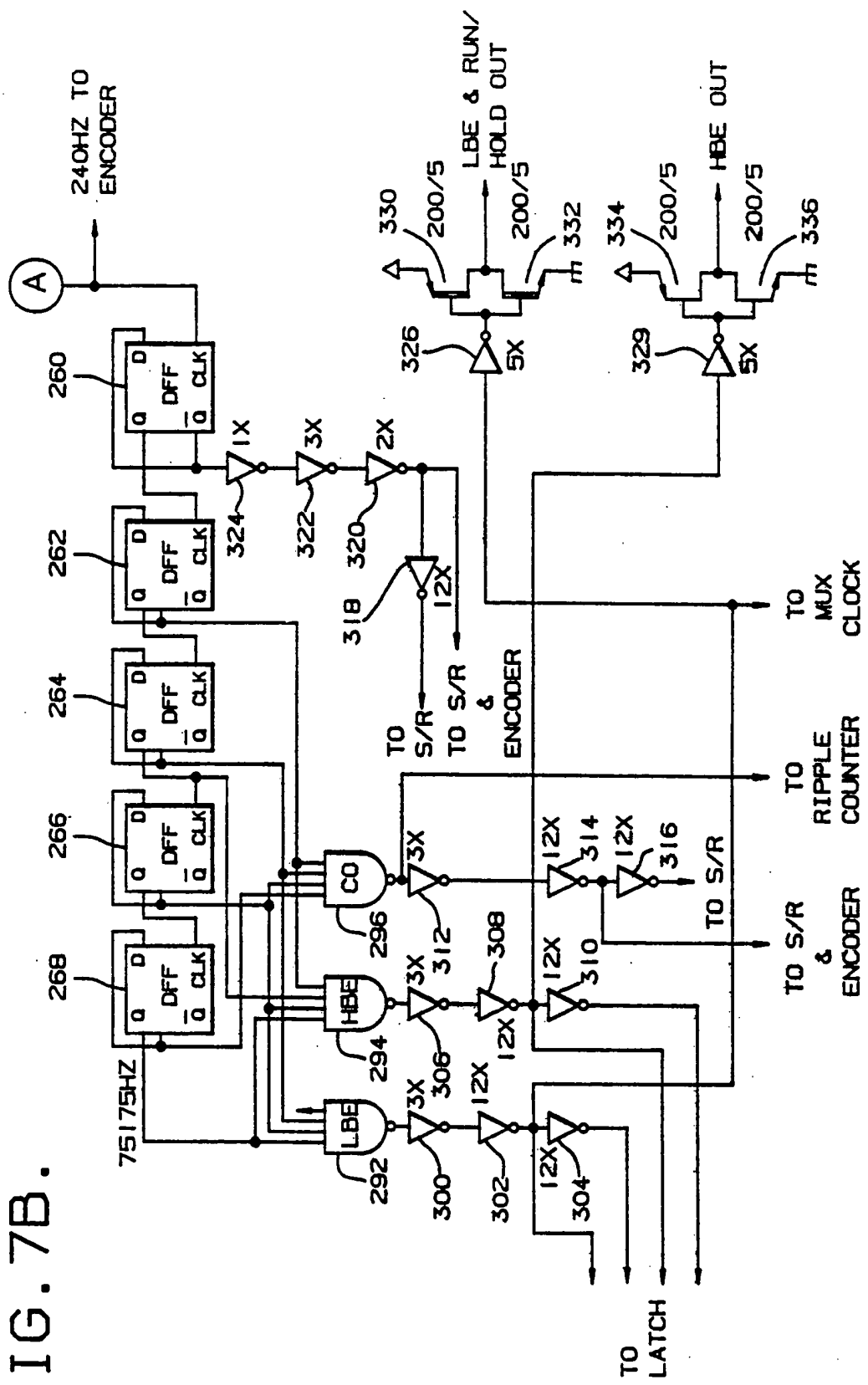

240HZ TO ENCODER
A
260
262
264
266
268
DFF
D
Q
CLK
75175HZ
1X
3X
2X
12X
324
322
320
318
CO
HBE
LBE
296
294
292
3X
12X
312
308
306
310
300
302
304
314
316
TO S/R
TO S/R & ENCODER
TO RIPPLE COUNTER
TO MUX CLOCK
TO S/R & ENCODER
TO LATCH
330
332
334
336
200/5
LBE & RUN/ HOLD OUT
HBE OUT
326
329
5X

FIG. 7B.

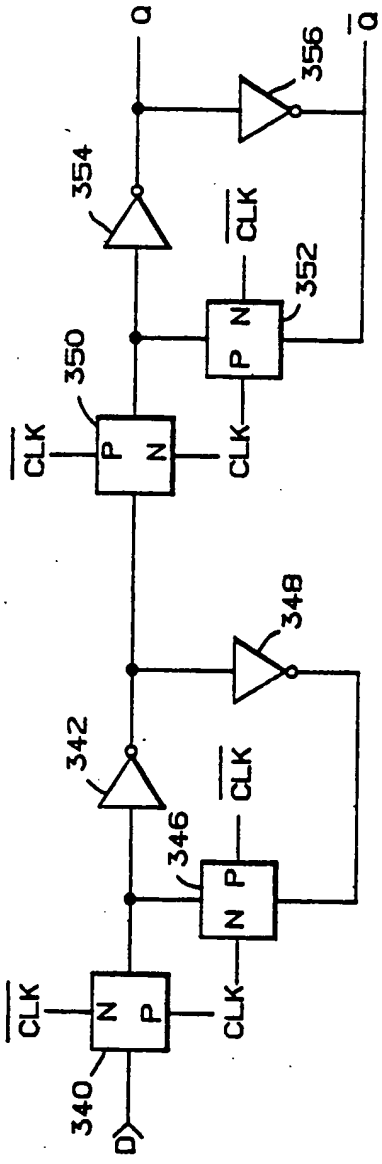

Q
$\overline{Q}$
356
354
$\overline{CLK}$
352
350
$\overline{CLK}$
CLK
P
N
348
342
346
340
D

FIG. 8.

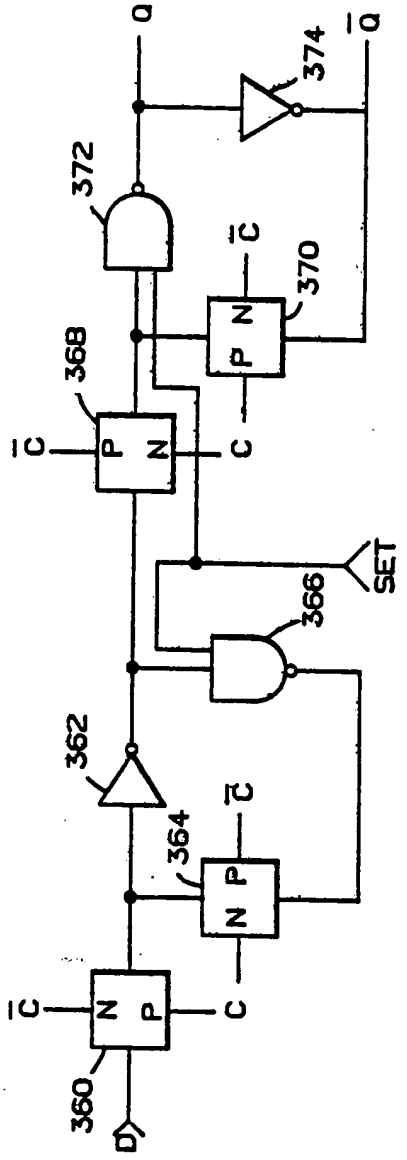

Q
$\overline{Q}$
374
372
$\overline{C}$
370
368
C
SET
366
362
364
360
D

FIG. 9.

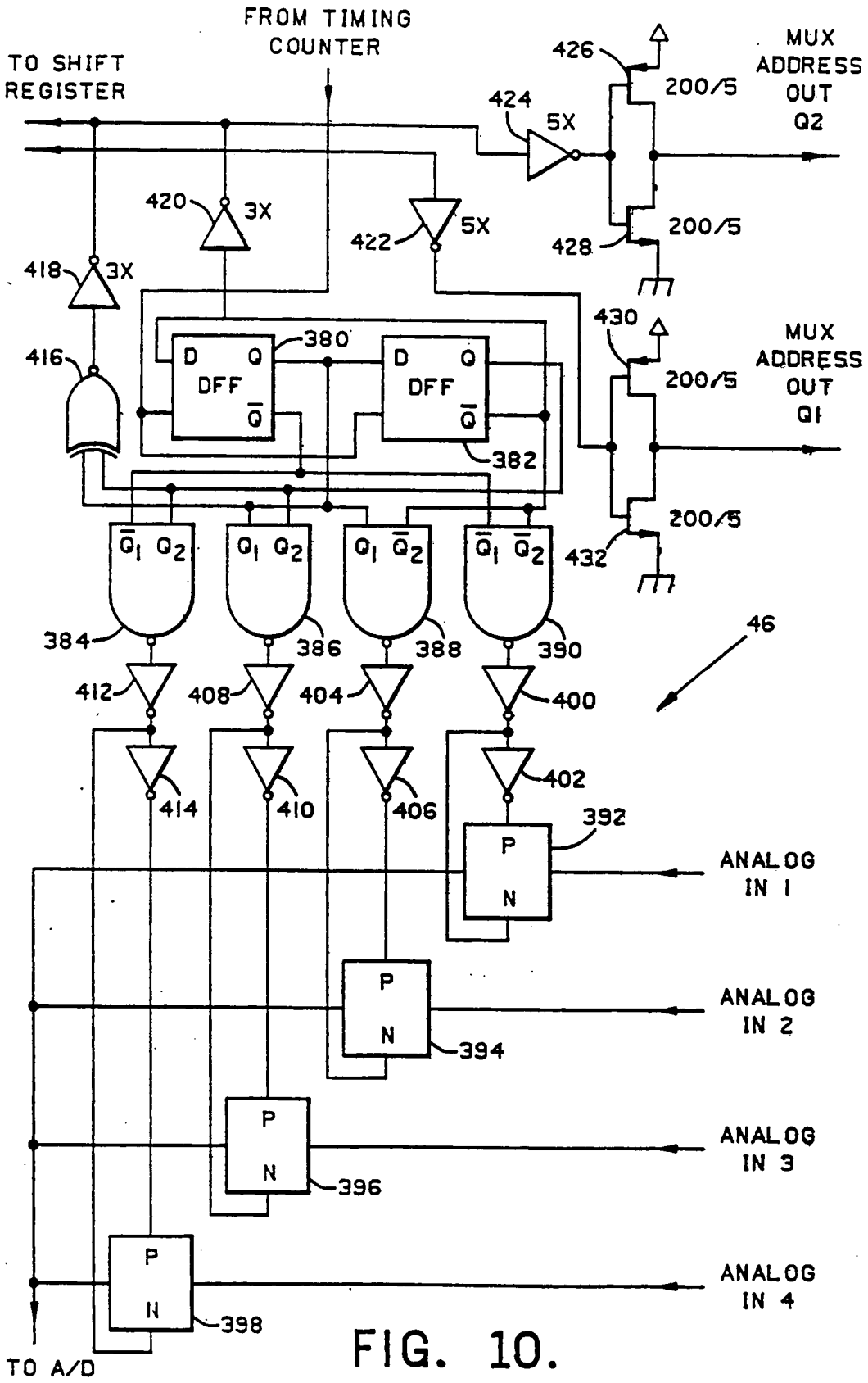

FROM TIMING COUNTER
TO SHIFT REGISTER
MUX ADDRESS OUT Q2
MUX ADDRESS OUT Q1
426
424
5X
200/5
420
3X
422
5X
428
418
3X
430
416
D Q
DFF
Q
380
382
432
$\bar{Q}_1$ Q_2
Q_1 Q_2
Q_1 $\bar{Q}_2$
$\bar{Q}_1$ $\bar{Q}_2$
384
386
388
390
46
412
408
404
400
414
410
406
402
392
P
N
ANALOG IN 1
ANALOG IN 2
394
ANALOG IN 3
396
ANALOG IN 4
398
TO A/D

FIG. 10.

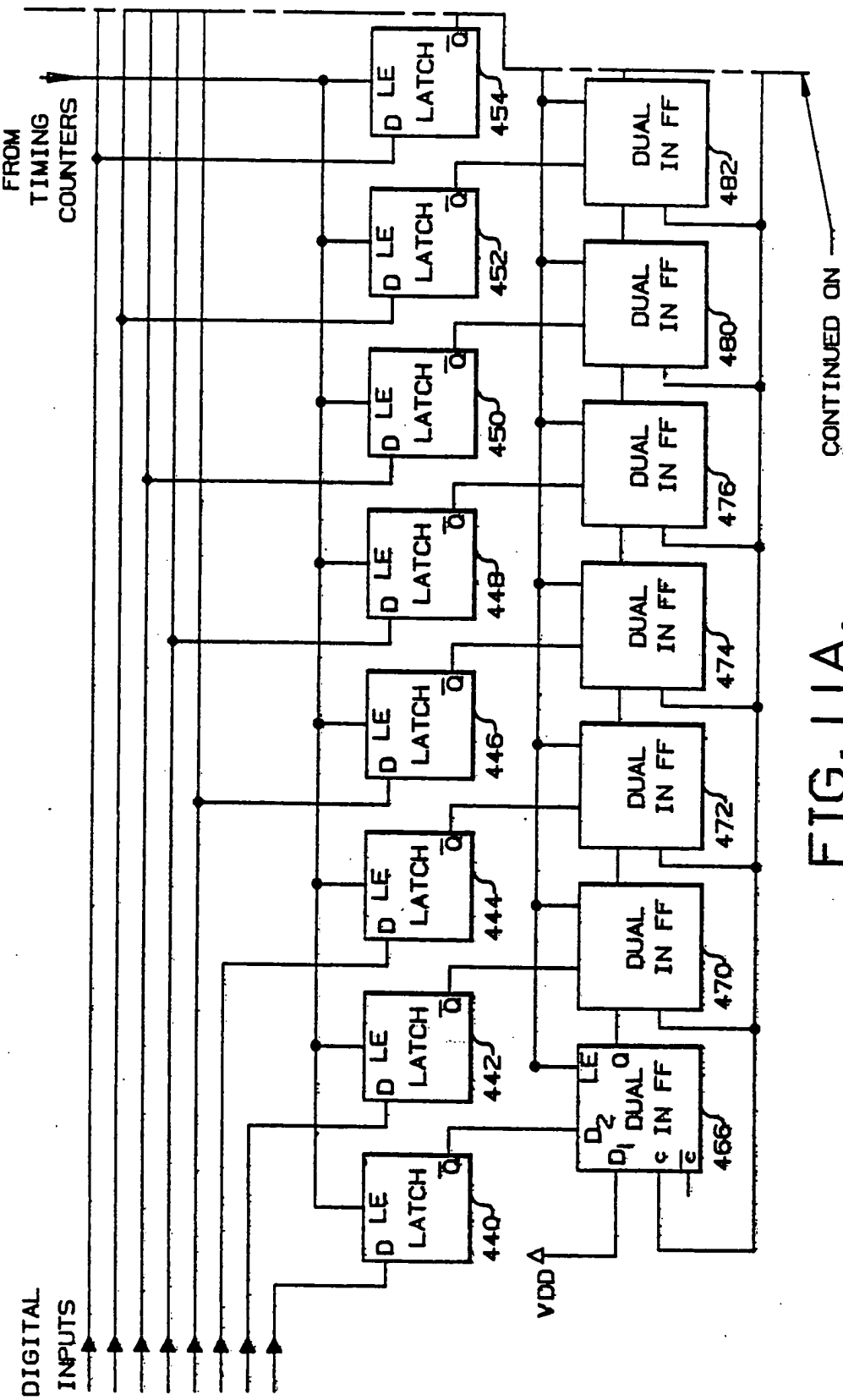

LOW BYTE ENABLE FROM TIMING COUNTERS
DIGITAL INPUTS
VDD
D LE LATCH Q
454
452
450
448
446
444
442
440
DUAL IN FF
482
480
476
474
472
470
466
CONTINUED ON FIG. 11B.

FIG. 11A.

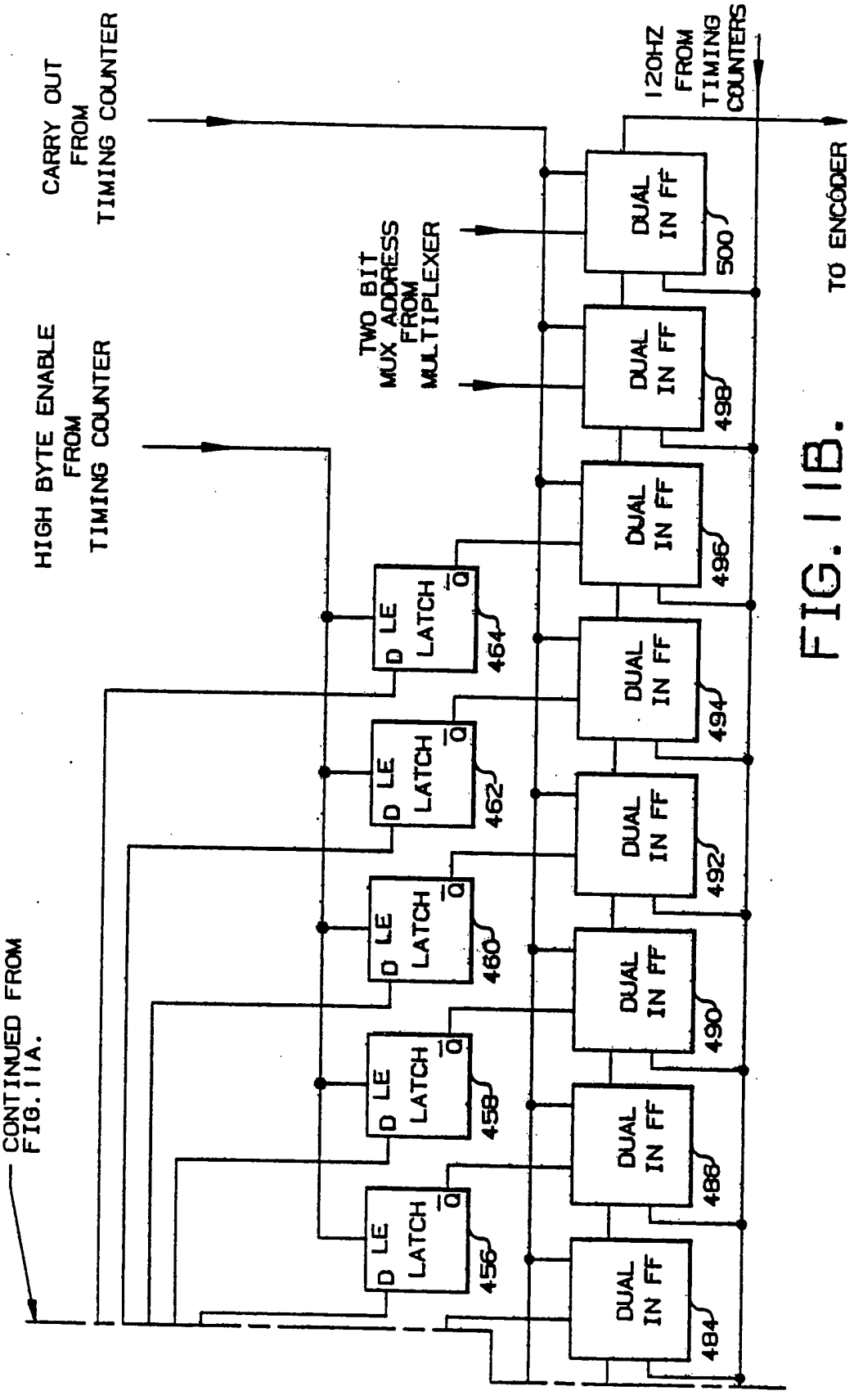

CONTINUED FROM FIG. IIA.
HIGH BYTE ENABLE FROM TIMING COUNTER
CARRY OUT FROM TIMING COUNTER
TWO BIT MUX ADDRESS FROM MULTIPLEXER
120HZ FROM TIMING COUNTERS
TO ENCODER
D LE LATCH Q
456
458
460
462
464
DUAL IN FF
484
488
490
492
494
496
498
500

FIG. IIB.

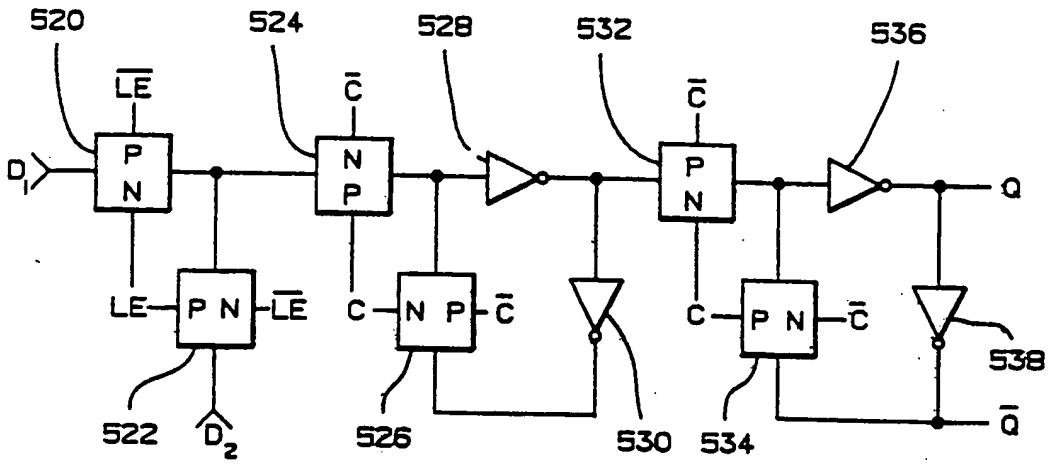

520
524
528
532
536
LE
C̄
C̄
C̄
D1
P
N
N
P
P
N
Q
LE
P N
LE
C
N P
C̄
C
P N
C̄
538
Q̄
522
D2
526
530
534

FIG. 13.

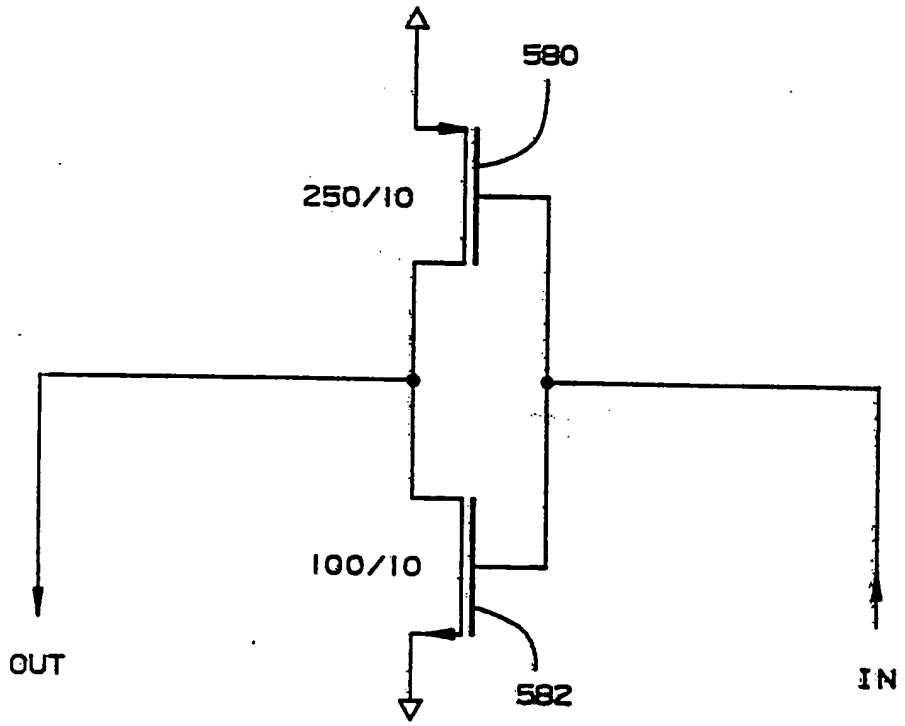

580
250/10
100/10
OUT
582
IN
58

FIG. 17.

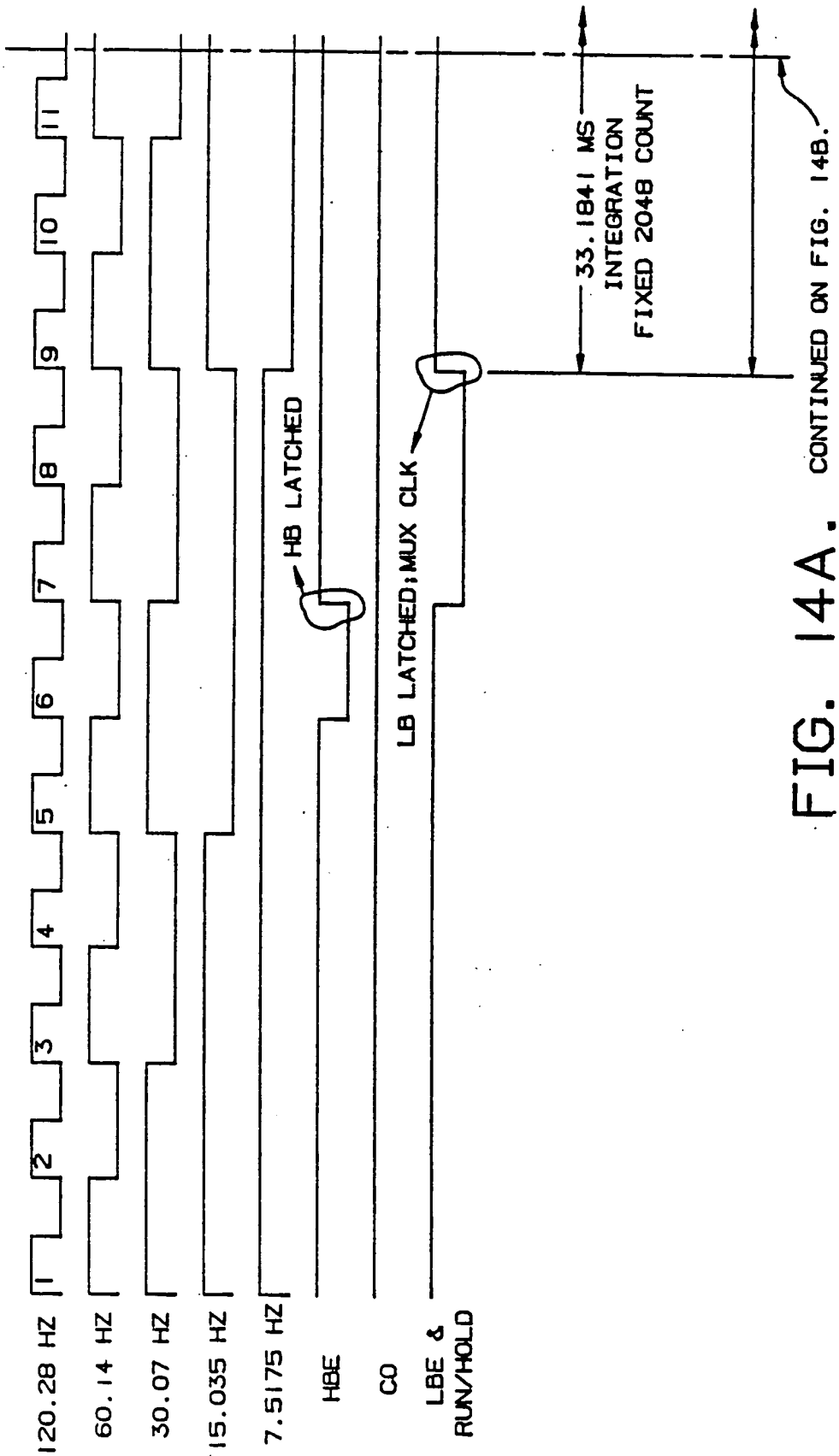

120.28 HZ
60.14 HZ
30.07 HZ
15.035 HZ
7.5175 HZ
HBE
CO
LBE & RUN/HOLD
1
2
3
4
5
6
7
8
9
10
11
HB LATCHED
LB LATCHED; MUX CLK
33.1841 MS INTEGRATION FIXED 2048 COUNT
CONTINUED ON FIG. 14B.

FIG. 14A.

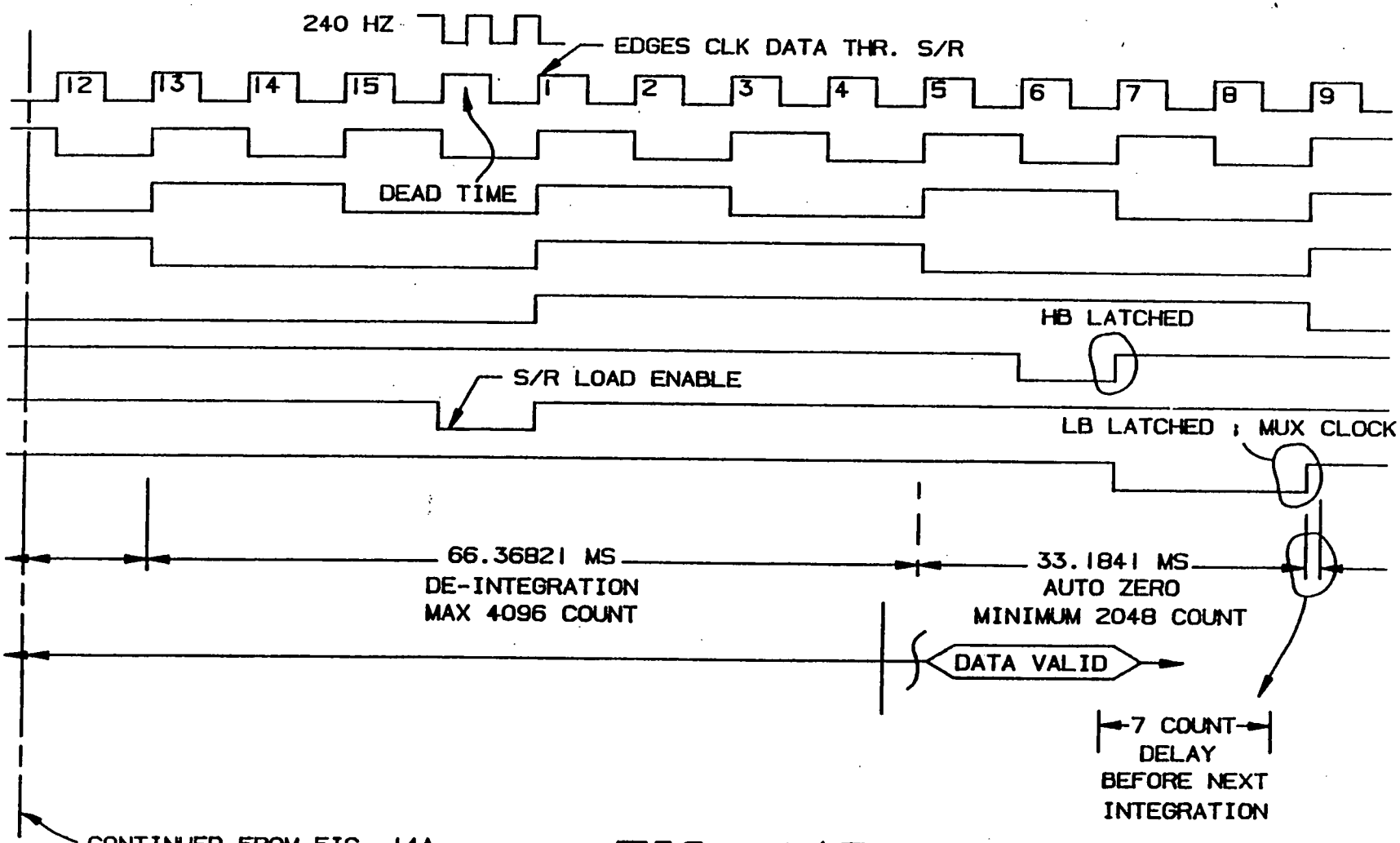

240 HZ
EDGES CLK DATA THR. S/R
12
13
14
15
1
2
3
4
5
6
7
8
9
DEAD TIME
HB LATCHED
S/R LOAD ENABLE
LB LATCHED ; MUX CLOCK
66.36821 MS
DE-INTEGRATION
MAX 4096 COUNT
33.1841 MS
AUTO ZERO
MINIMUM 2048 COUNT
DATA VALID
7 COUNT
DELAY
BEFORE NEXT
INTEGRATION
CONTINUED FROM FIG. 14A.
CONVERSION=113.422 μs

FIG. 14B.

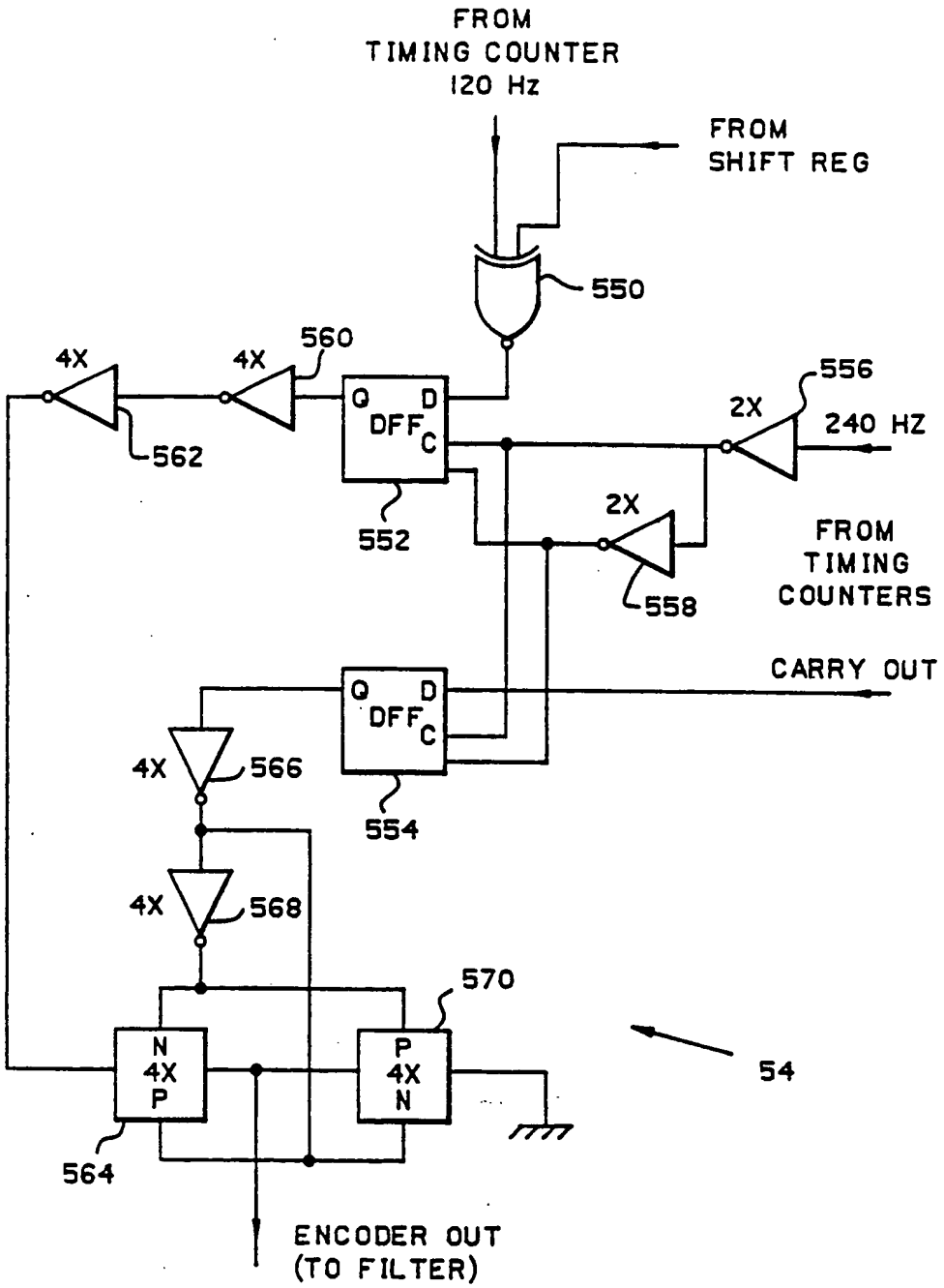

FROM
TIMING COUNTER
120 Hz
FROM
SHIFT REG
550
560
4X
4X
562
Q D
DFF
C
552
556
2X
240 HZ
2X
558
FROM
TIMING
COUNTERS
CARRY OUT
Q D
DFF
C
554
4X
566
4X
568
570
N
4X
P
P
4X
N
564
54
ENCODER OUT
(TO FILTER)

FIG. 15.

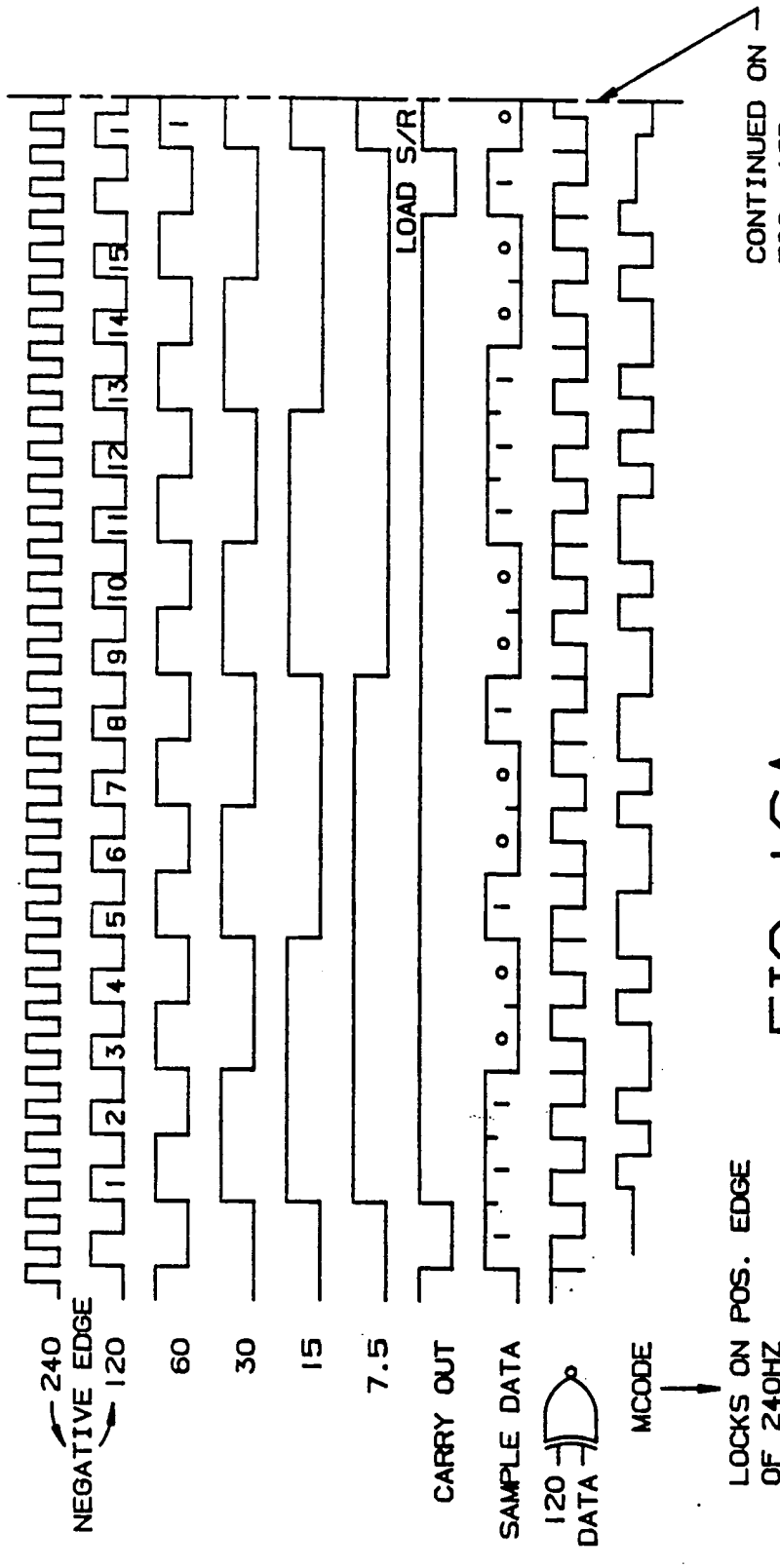

240
NEGATIVE EDGE
120
60
30
15
7.5
LOAD S/R
CARRY OUT
SAMPLE DATA
120 DATA
MCODE
LOCKS ON POS. EDGE OF 240HZ
CONTINUED ON FIG. 16B.

FIG. 16A.

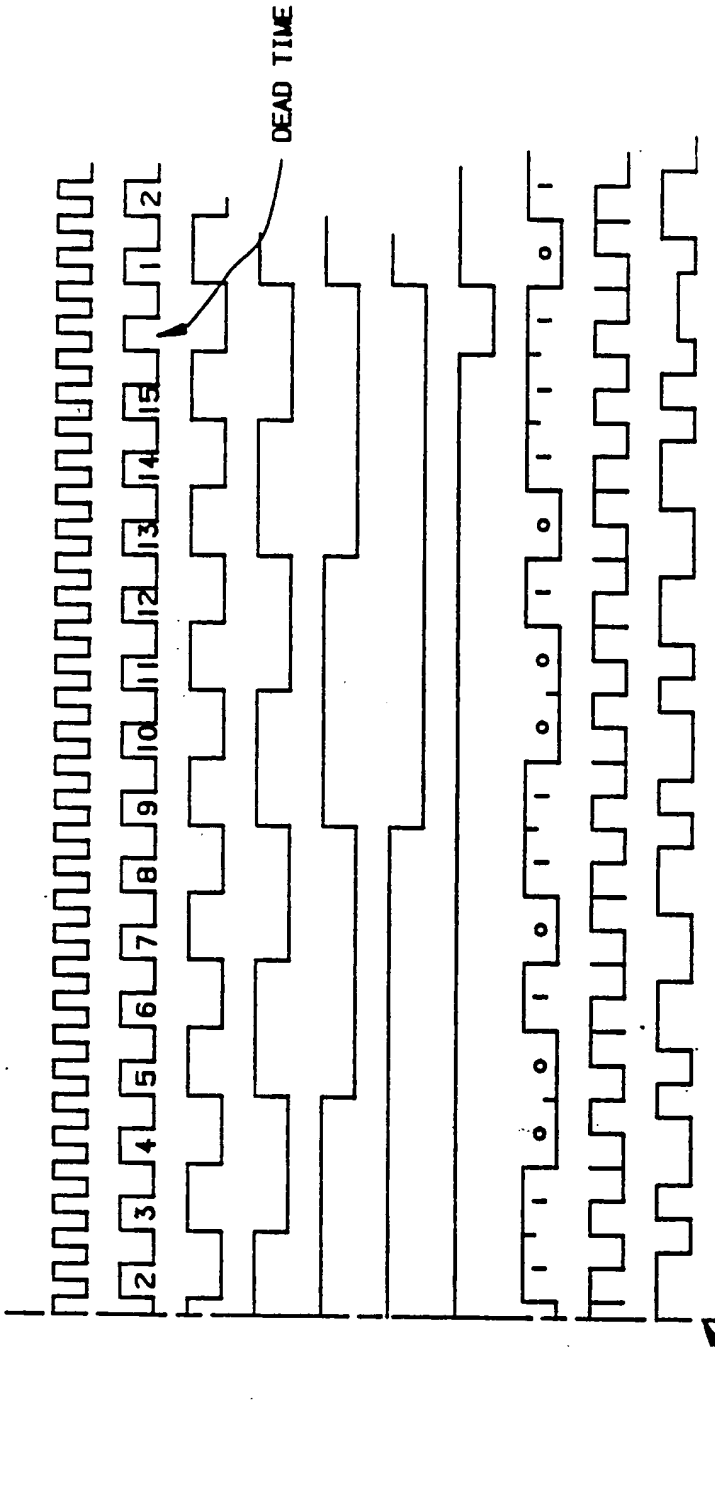


FIG. 16B.

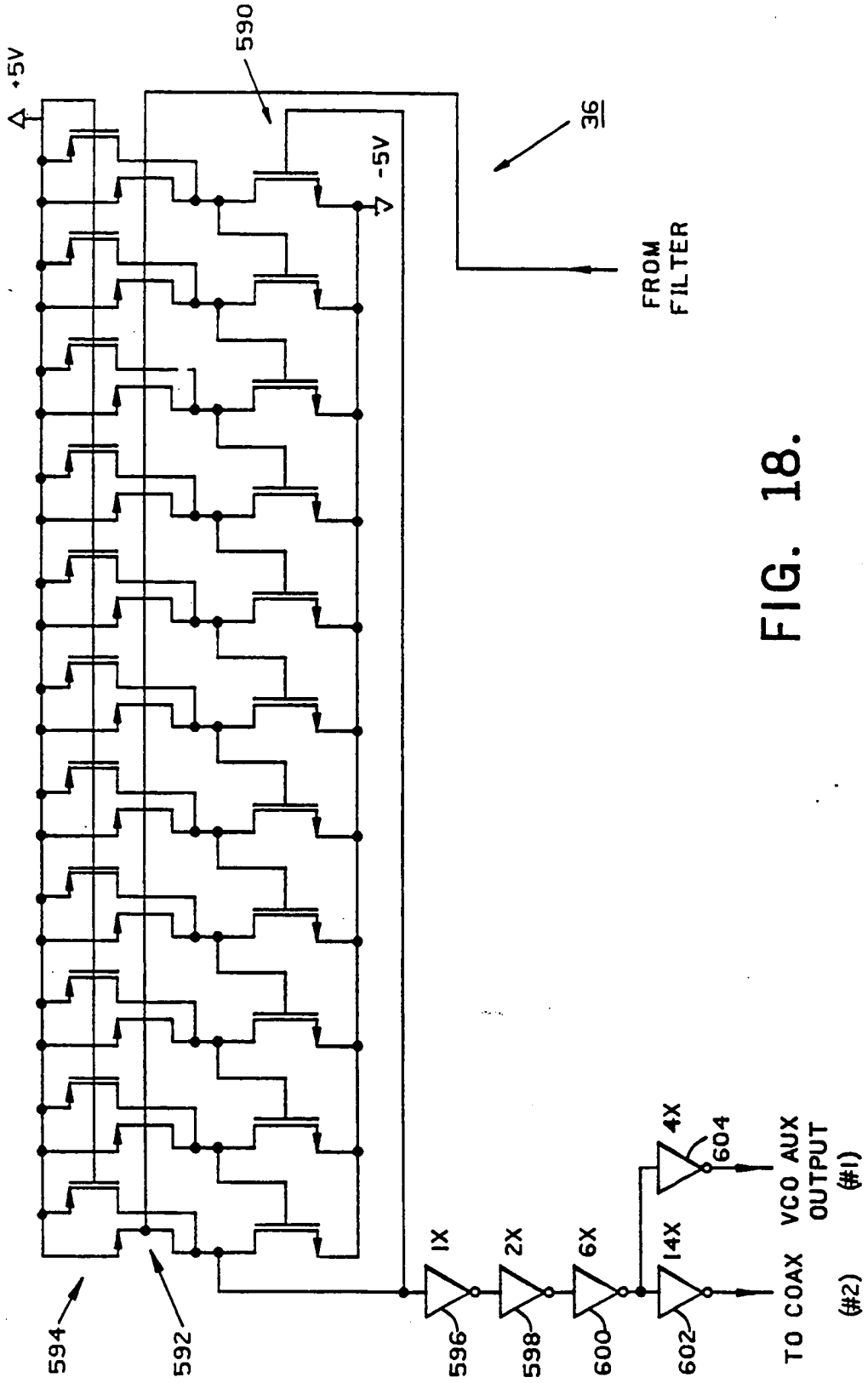

+5V
590
-5V
36
FROM FILTER
1X
2X
6X
14X
4X
604
VCO AUX OUTPUT (#1)
TO COAX (#2)
594
592
596
598
600
602

FIG. 18.

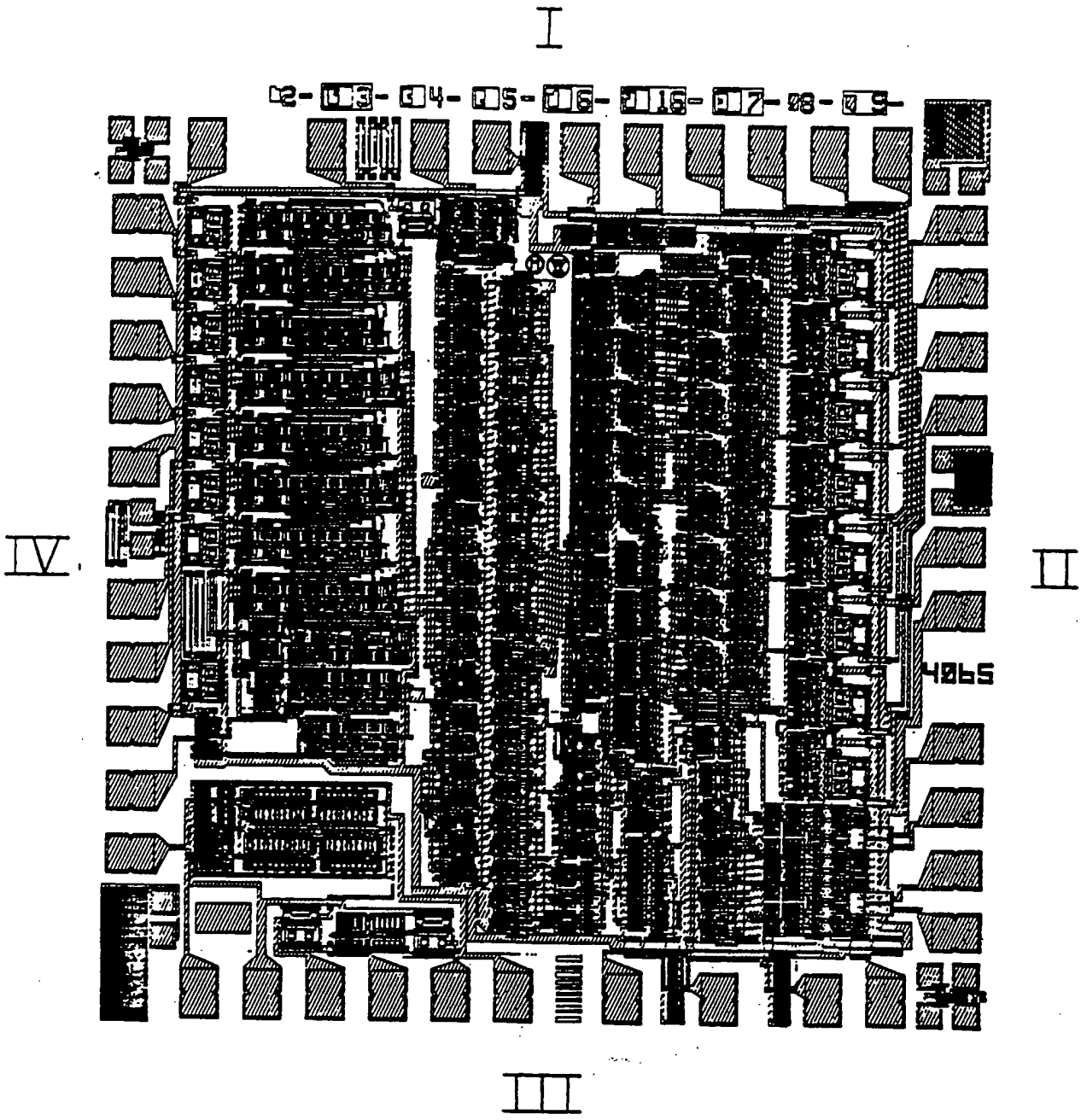


FIG. 20.

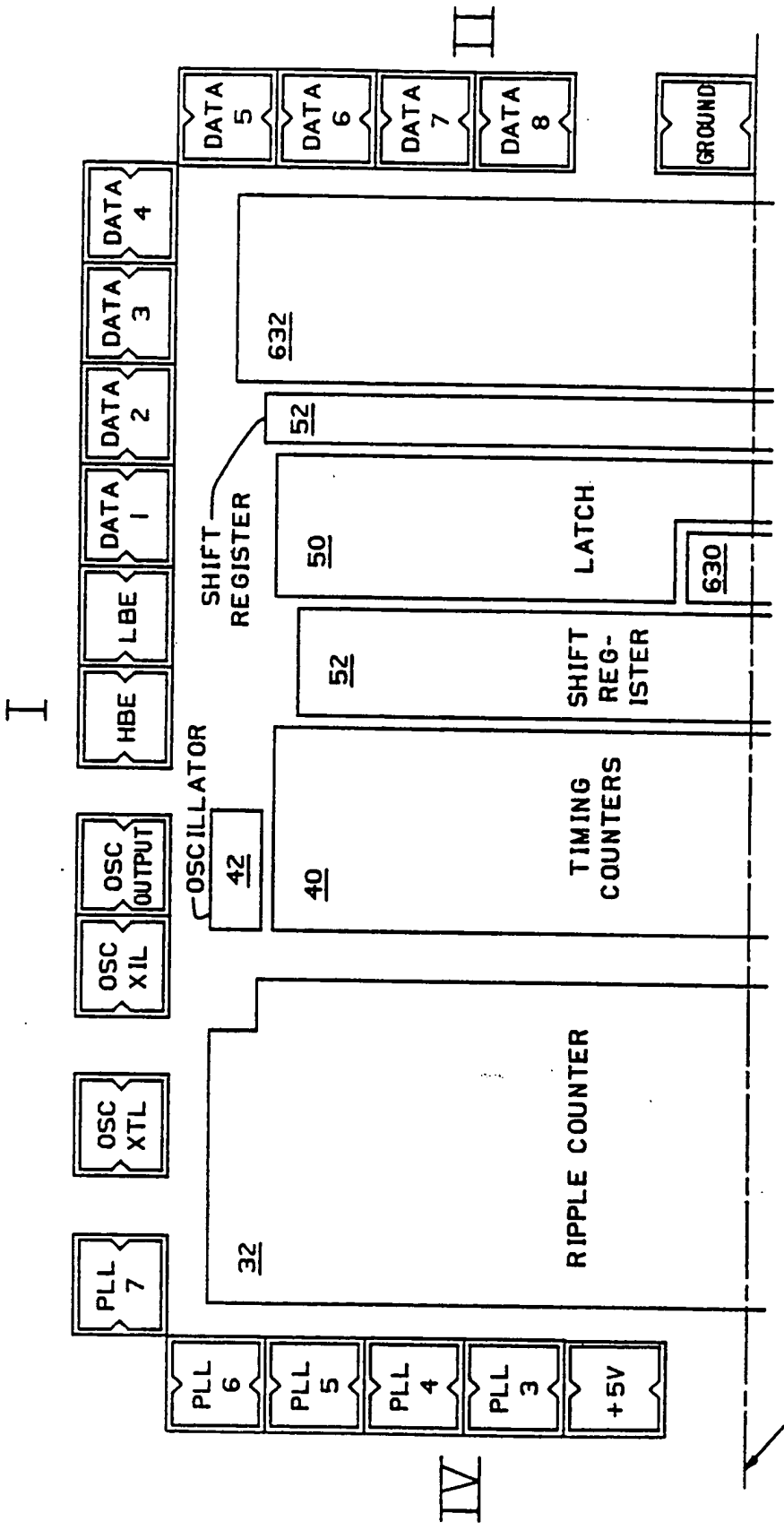

I
II
IV
DATA 5
DATA 6
DATA 7
DATA 8
GROUND
DATA 4
DATA 3
DATA 2
DATA 1
LBE
HBE
632
52
SHIFT REGISTER
50
LATCH
630
52
SHIFT REG-ISTER
OSC OUTPUT
OSC XIL
OSCILLATOR
42
40
TIMING COUNTERS
OSC XTL
32
RIPPLE COUNTER
PLL 7
PLL 6
PLL 5
PLL 4
PLL 3
+5V
CONTINUED ON FIG. 21B.

FIG. 21A.

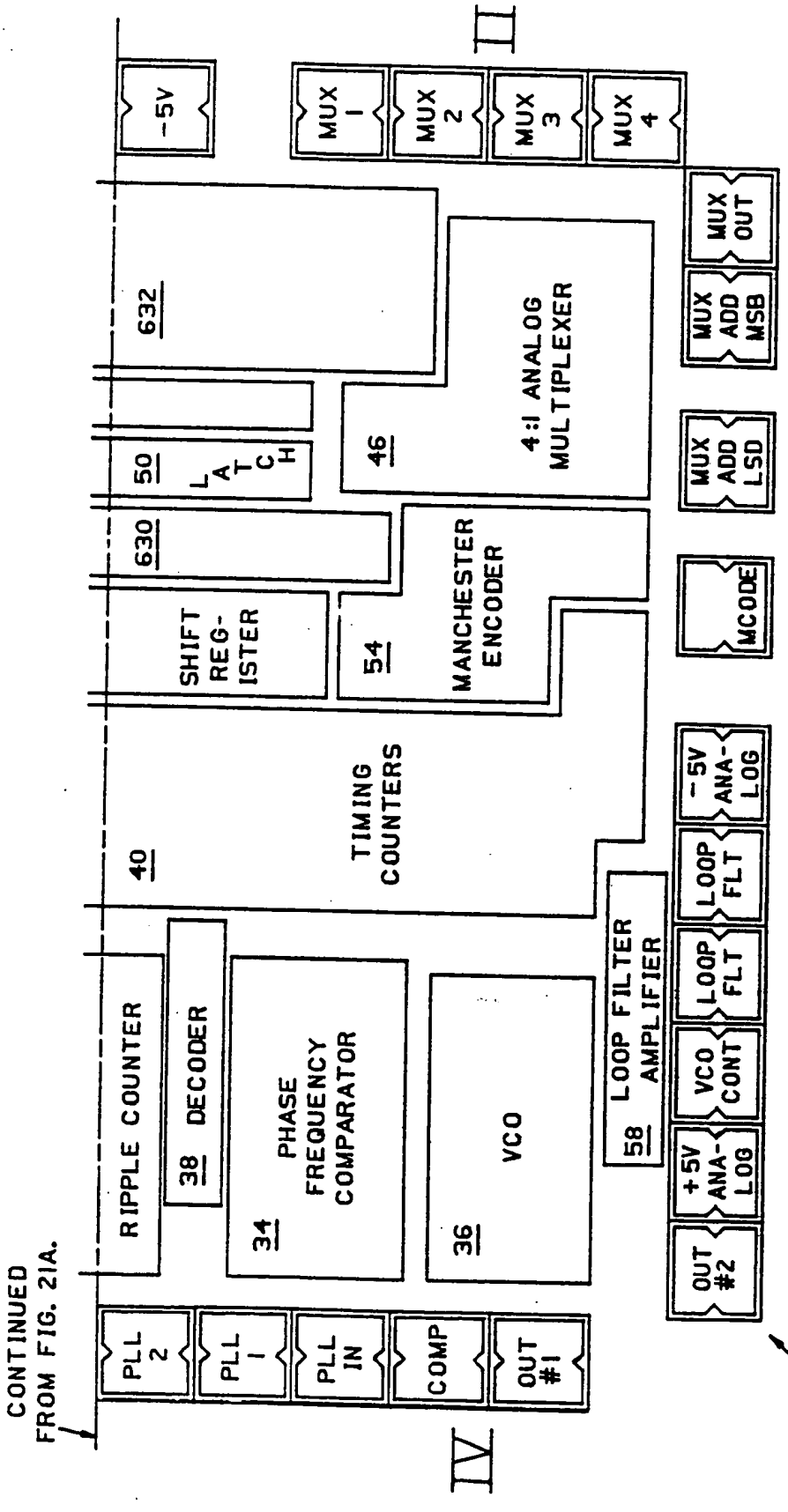

CONTINUED FROM FIG. 21A.
PLL 2
PLL 1
PLL IN
COMP
OUT #1
RIPPLE COUNTER
38 DECODER
34 PHASE FREQUENCY COMPARATOR
36 VCO
58 LOOP FILTER AMPLIFIER
OUT #2
+5V ANA-LOG
VCO CONT
LOOP FLT
LOOP FLT
-5V ANA-LOG
40 TIMING COUNTERS
SHIFT REG-ISTER
630
54 MANCHESTER ENCODER
MCODE
50 LATCH
632
46 4:1 ANALOG MULTIPLEXER
-5V
MUX 1
MUX 2
MUX 3
MUX 4
MUX ADD LSD
MUX ADD MSB
MUX OUT
IV
III
II
30

FIG. 21B.

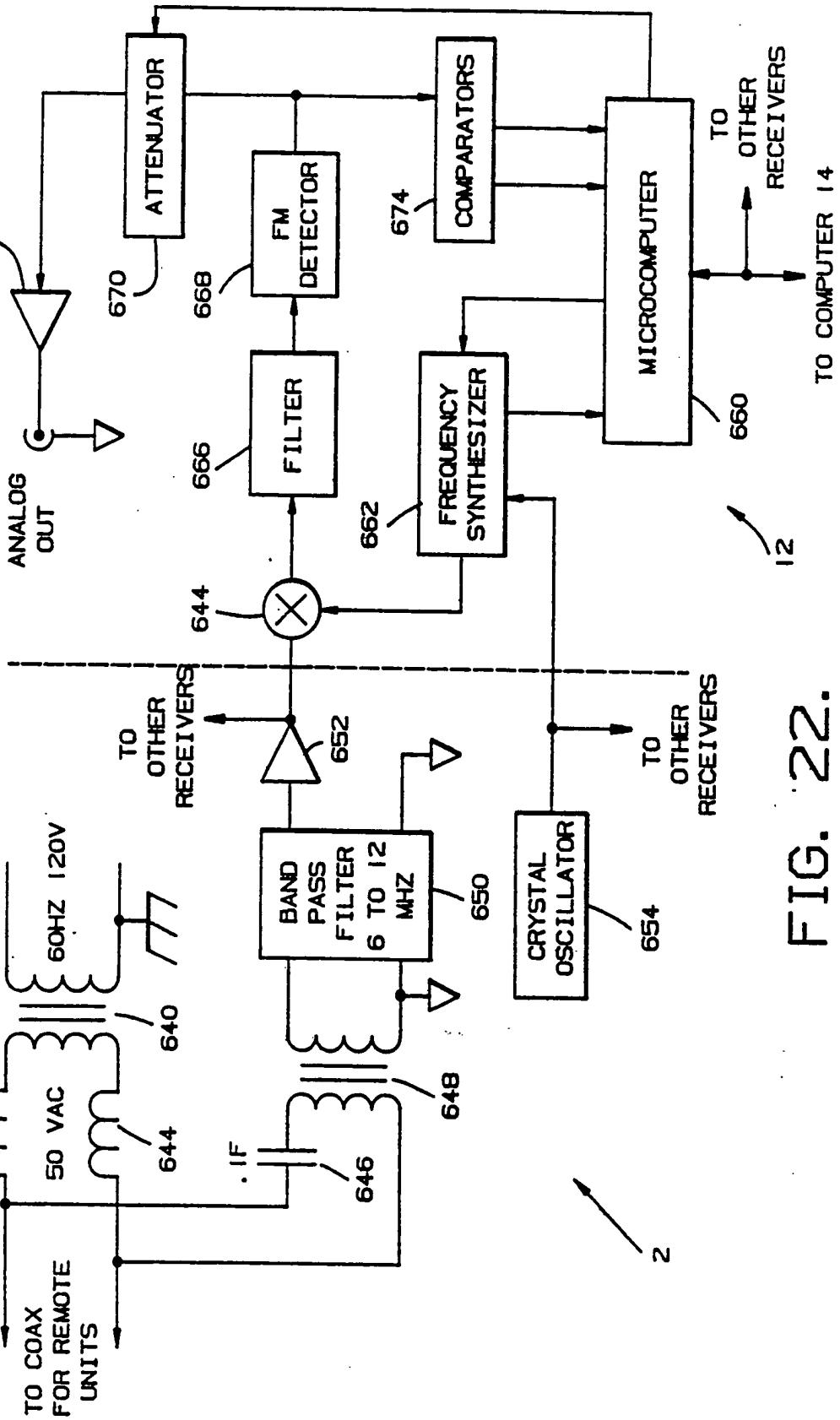

TO COAX FOR REMOTE UNITS
50 VAC
644
642
60HZ 120V
640
.1F
646
648
BAND PASS FILTER 6 TO 12 MHZ
650
CRYSTAL OSCILLATOR
654
TO OTHER RECEIVERS
652
TO OTHER RECEIVERS
644
FREQUENCY SYNTHESIZER
662
FILTER
666
FM DETECTOR
668
ATTENUATOR
670
672
ANALOG OUT
COMPARATORS
674
MICROCOMPUTER
660
TO OTHER RECEIVERS
TO COMPUTER 14
12
2

FIG. 22.

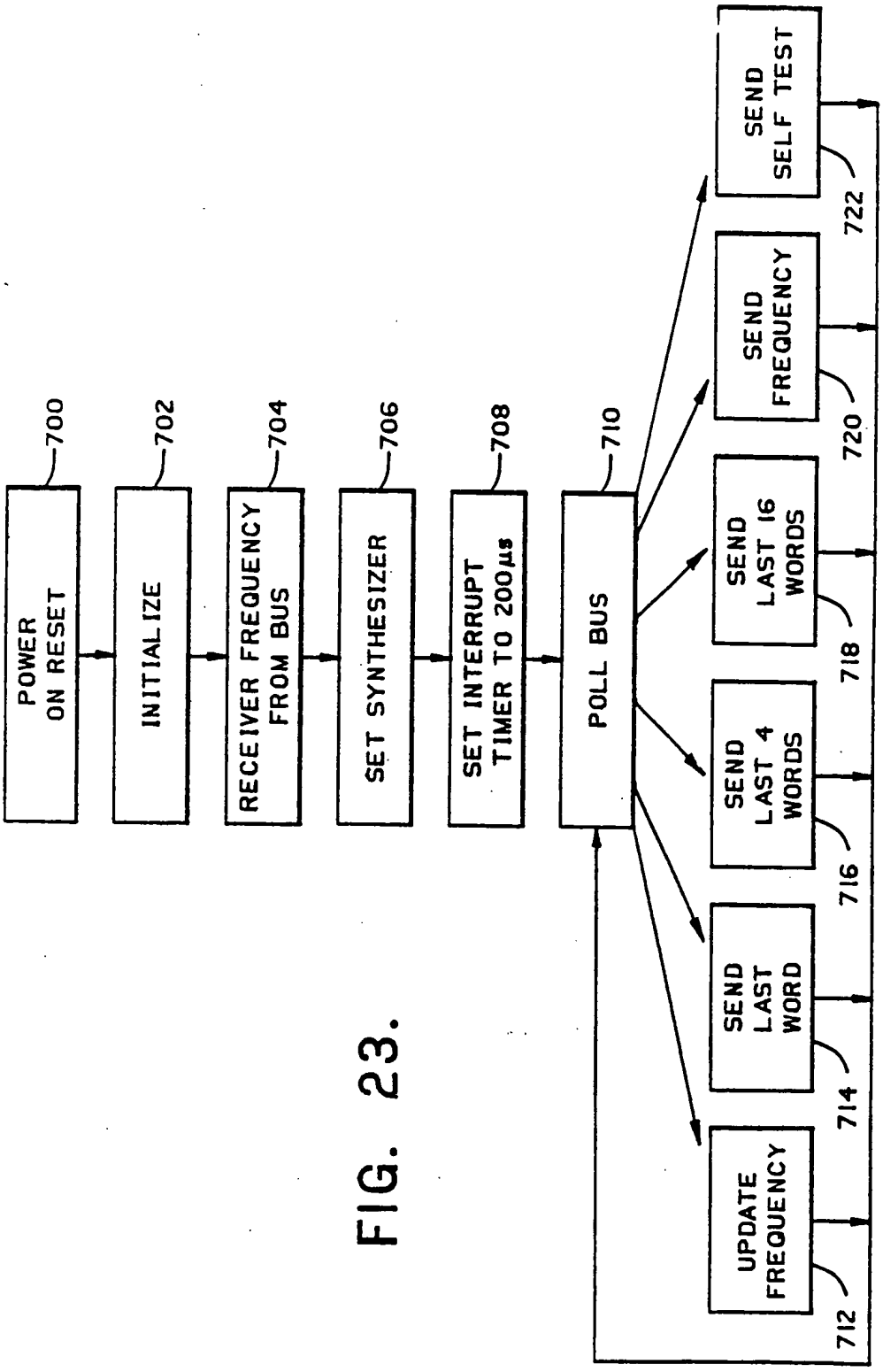

POWER ON RESET
700
INITIALIZE
702
RECEIVER FREQUENCY FROM BUS
704
SET SYNTHESIZER
706
SET INTERRUPT TIMER TO 200μs
708
POLL BUS
710
SEND SELF TEST
722
SEND FREQUENCY
720
SEND LAST 16 WORDS
718
SEND LAST 4 WORDS
716
SEND LAST WORD
714
UPDATE FREQUENCY
712

FIG. 23.

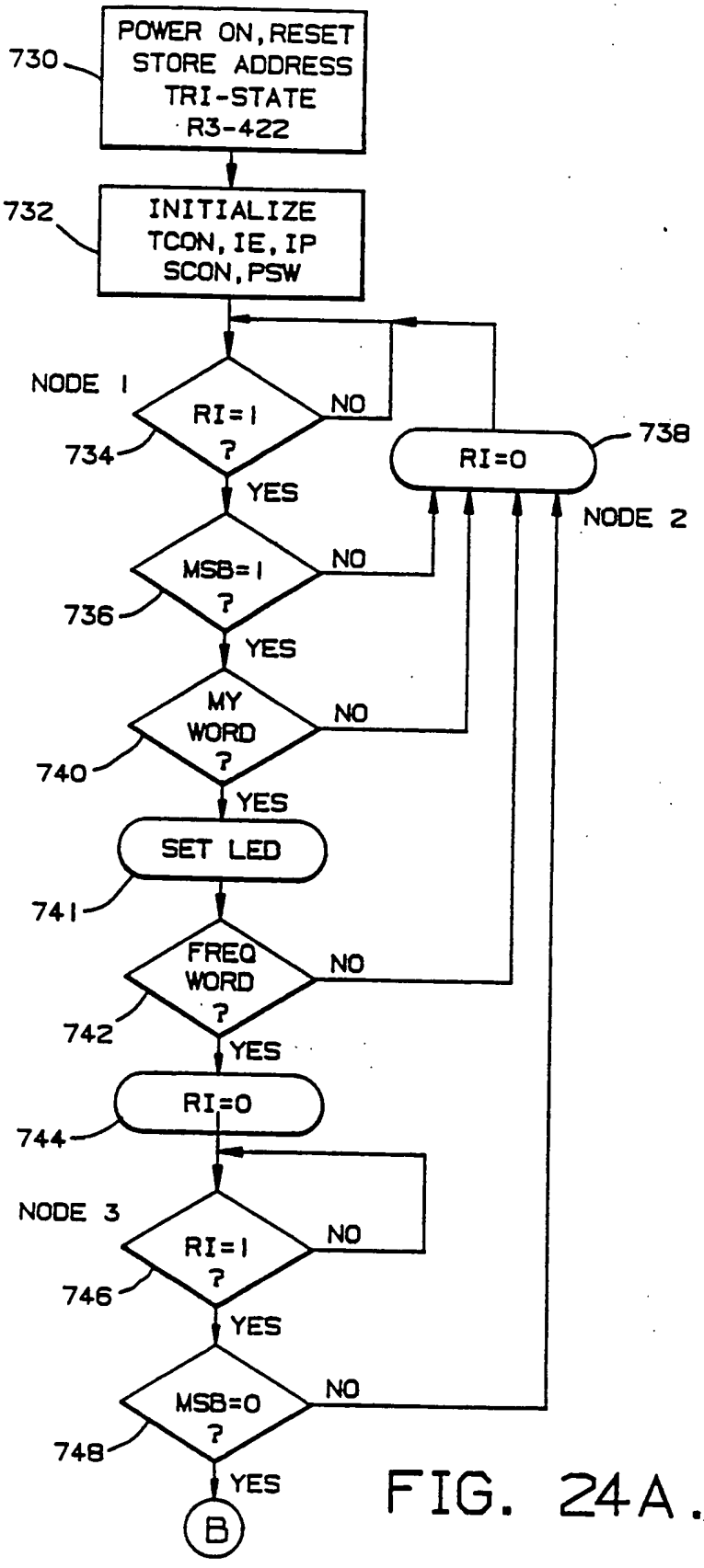

POWER ON, RESET
STORE ADDRESS
TRI-STATE
R3-422
730
INITIALIZE
TCON, IE, IP
SCON, PSW
732
NODE 1
RI=1
?
734
NO
YES
RI=0
738
NODE 2
MSB=1
?
736
NO
YES
MY
WORD
?
740
NO
YES
SET LED
741
FREQ
WORD
?
742
NO
YES
RI=0
744
NODE 3
RI=1
?
746
NO
YES
MSB=0
?
748
NO
YES
B

FIG. 24A.

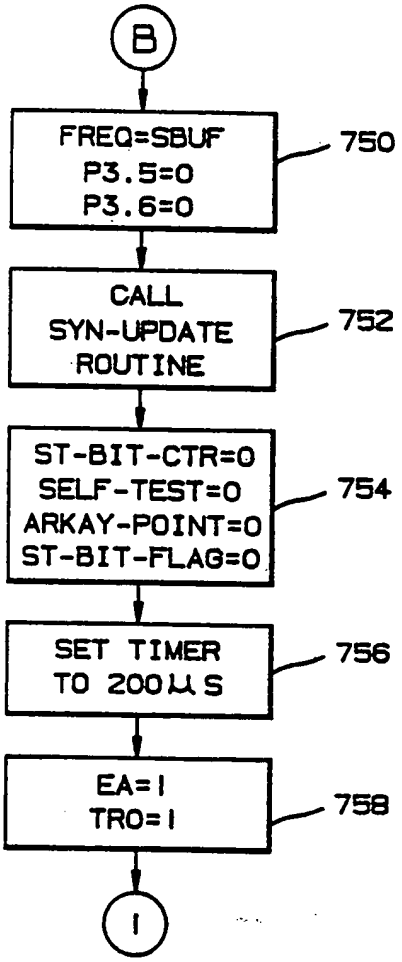

B
FREQ=SBUF
P3.5=0
P3.6=0
750
CALL
SYN-UPDATE
ROUTINE
752
ST-BIT-CTR=0
SELF-TEST=0
ARKAY-POINT=0
ST-BIT-FLAG=0
754
SET TIMER
TO 200μS
756
EA=1
TR0=1
758
1

FIG. 24B.

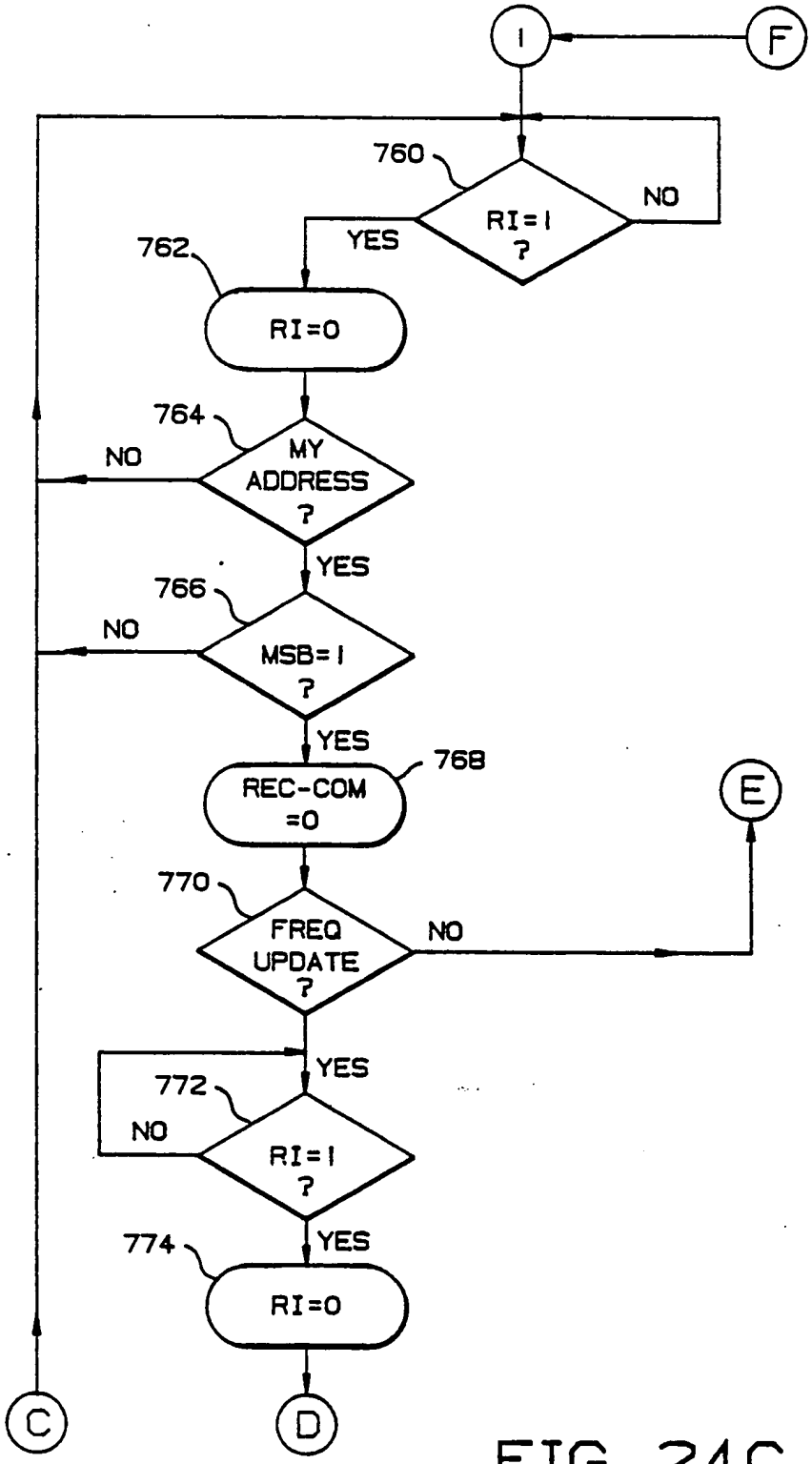

I
F
760
RI=1 ?
NO
YES
762
RI=0
764
MY ADDRESS ?
NO
YES
766
MSB=1 ?
NO
YES
768
REC-COM =0
E
770
FREQ UPDATE ?
NO
YES
772
RI=1 ?
NO
YES
774
RI=0
C
D

FIG. 24C.

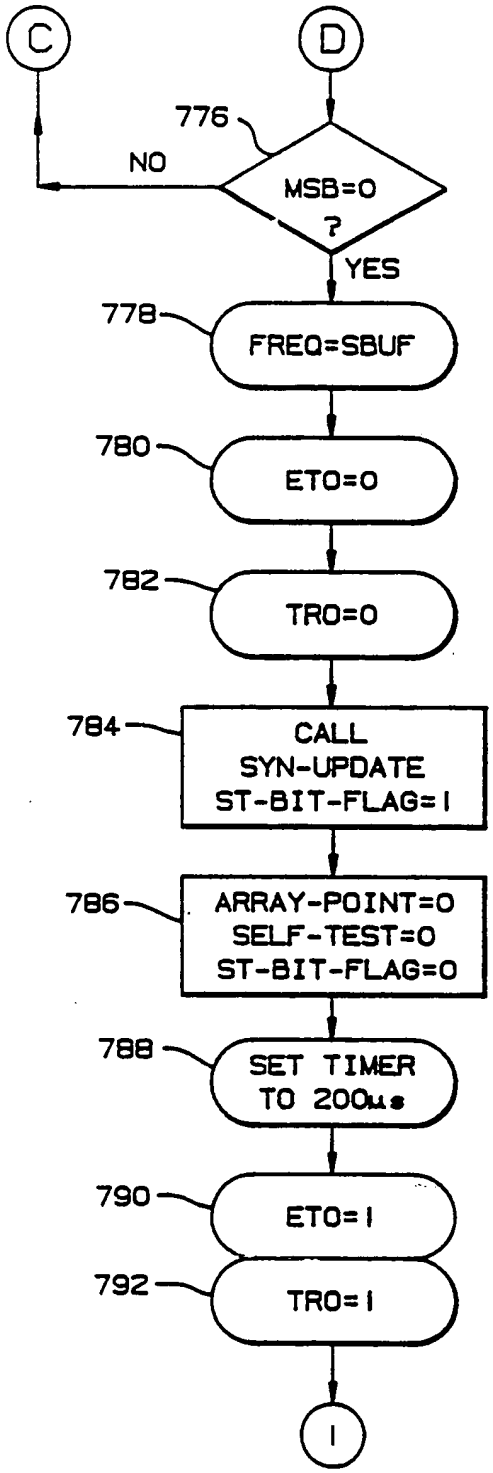

C
D
776
NO
MSB=0
?
YES
778
FREQ=SBUF
780
ETO=0
782
TRO=0
784
CALL
SYN-UPDATE
ST-BIT-FLAG=1
786
ARRAY-POINT=0
SELF-TEST=0
ST-BIT-FLAG=0
788
SET TIMER
TO 200μs
790
ETO=1
792
TRO=1
1

FIG. 24D.

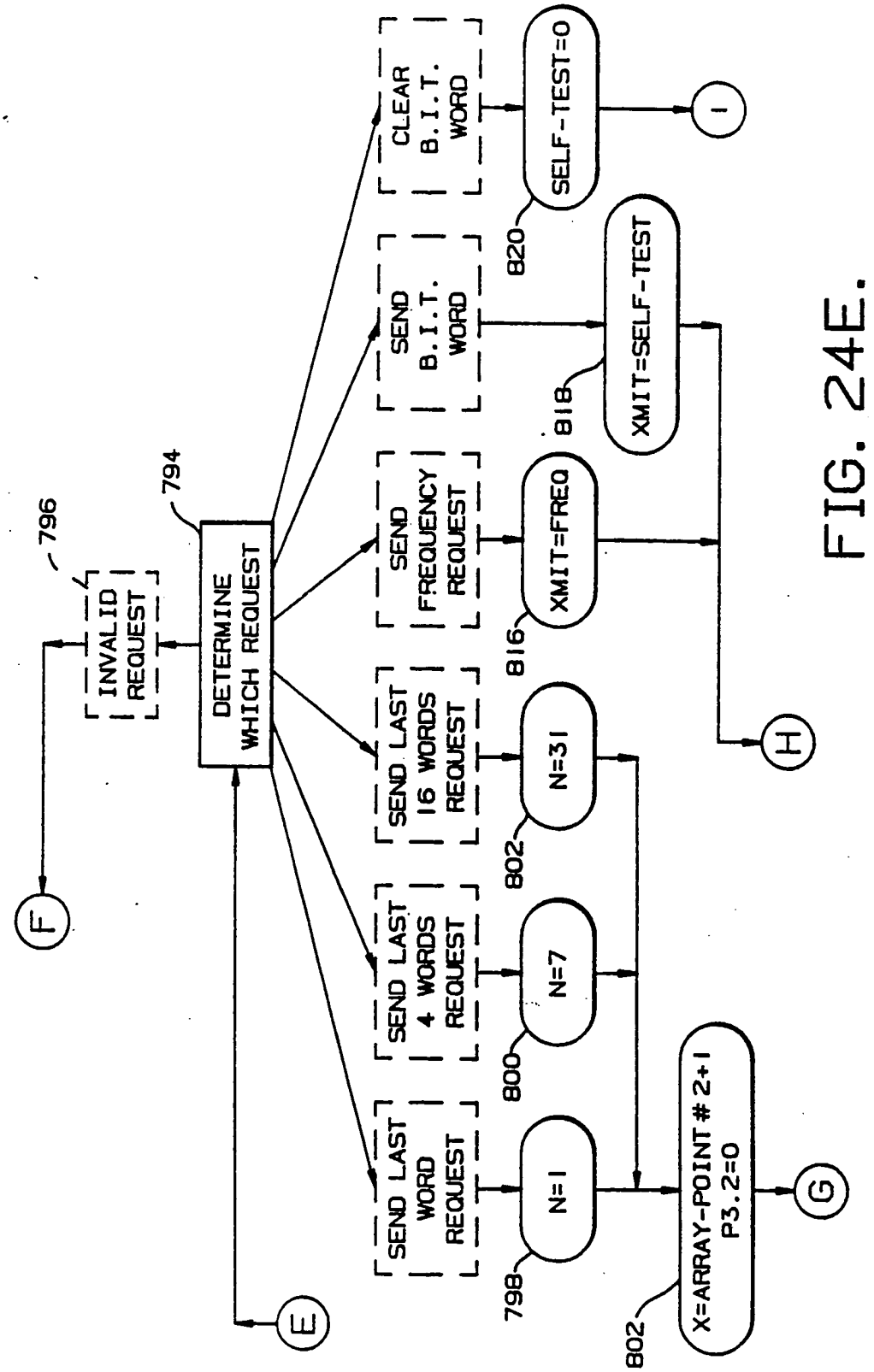

F
INVALID REQUEST
796
DETERMINE WHICH REQUEST
794
E
SEND LAST WORD REQUEST
SEND LAST 4 WORDS REQUEST
SEND LAST 16 WORDS REQUEST
SEND FREQUENCY REQUEST
SEND B.I.T. WORD
CLEAR B.I.T. WORD
N=1
798
N=7
800
N=31
802
XMIT=FREQ
816
XMIT=SELF-TEST
818
SELF-TEST=0
820
X=ARRAY-POINT # 2+1
P3.2=0
802
G
H
I

FIG. 24E.

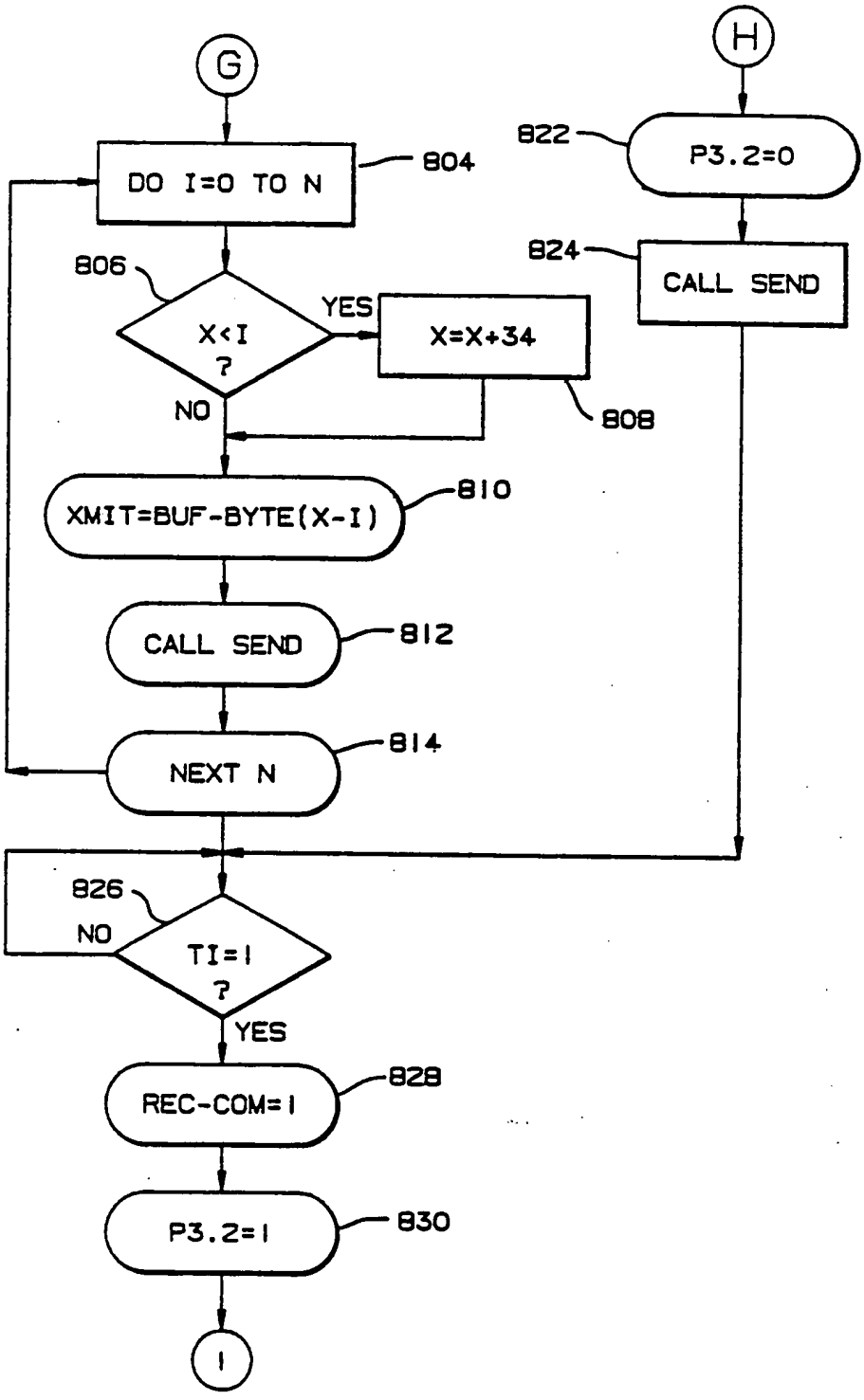

G
H
DO I=0 TO N
804
822
P3.2=0
824
CALL SEND
806
X<I
?
YES
X=X+34
808
NO
XMIT=BUF-BYTE(X-I)
810
CALL SEND
812
NEXT N
814
826
NO
TI=1
?
YES
REC-COM=1
828
P3.2=1
830
I

FIG. 24F.

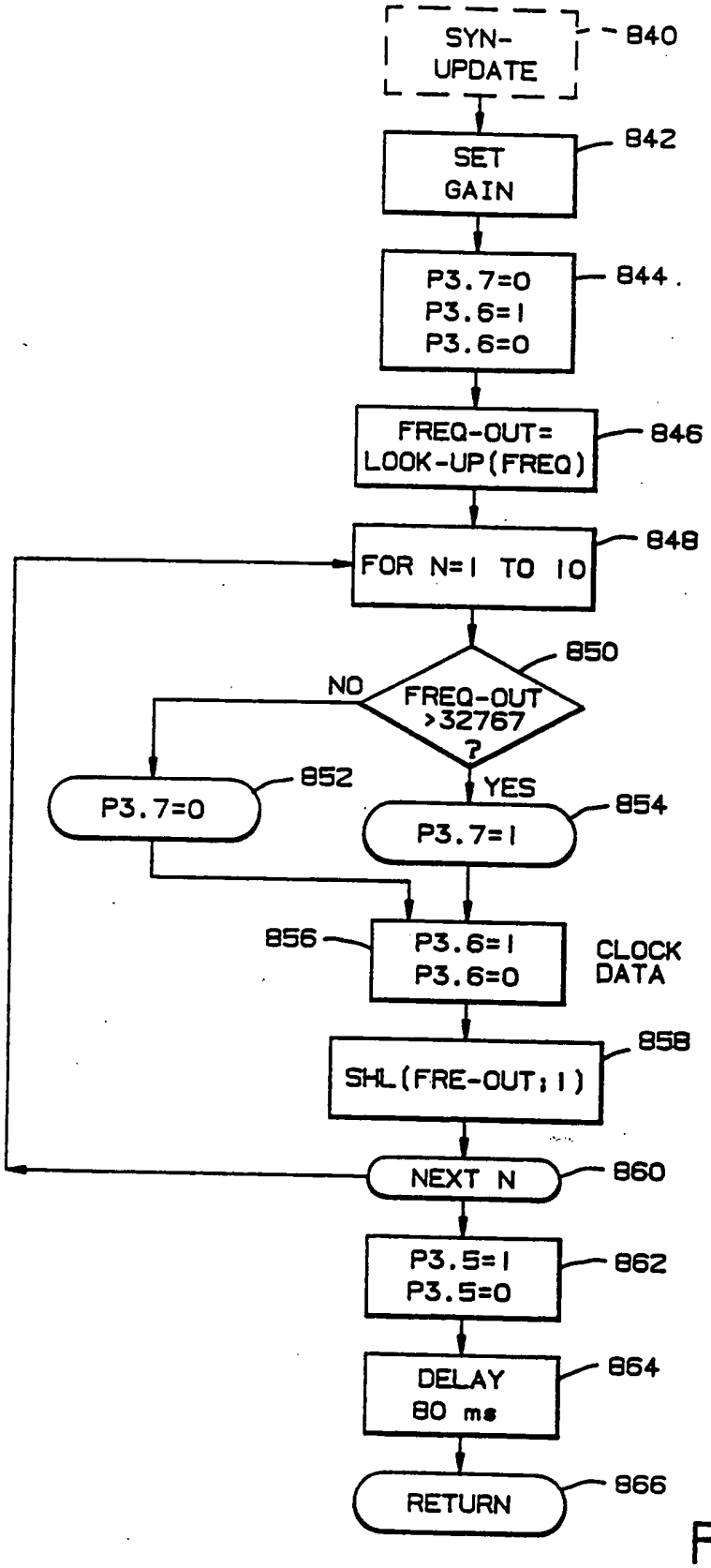

SYN-
UPDATE
840
SET
GAIN
842
P3.7=0
P3.6=1
P3.6=0
844
FREQ-OUT=
LOOK-UP(FREQ)
846
FOR N=1 TO 10
848
850
NO
FREQ-OUT
>32767
?
YES
852
P3.7=0
854
P3.7=1
856
P3.6=1
P3.6=0
CLOCK
DATA
858
SHL(FRE-OUT;1)
NEXT N
860
P3.5=1
P3.5=0
862
DELAY
80 ms
864
RETURN
866

FIG. 25.

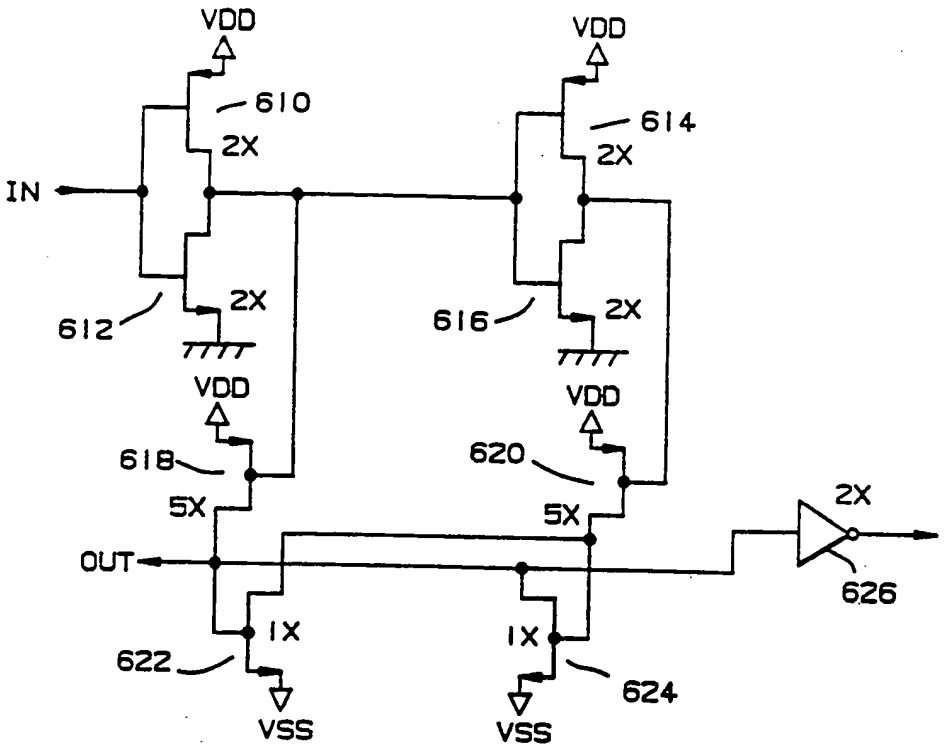

VDD
610
2X
IN
612
2X
VDD
618
5X
OUT
622
1X
VSS
VDD
614
2X
616
2X
VDD
620
5X
1X
624
VSS
2X
626

FIG. 19.

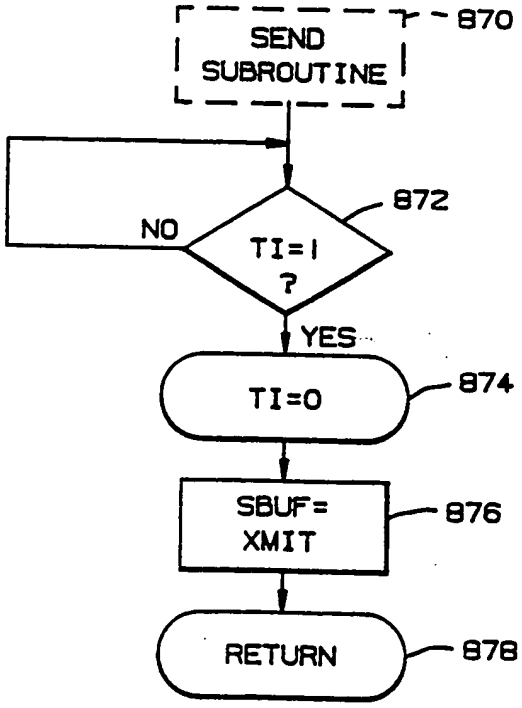

870
SEND
SUBROUTINE
872
NO
TI=1
?
YES
TI=0
874
SBUF=
XMIT
876
RETURN
878

FIG. 26.

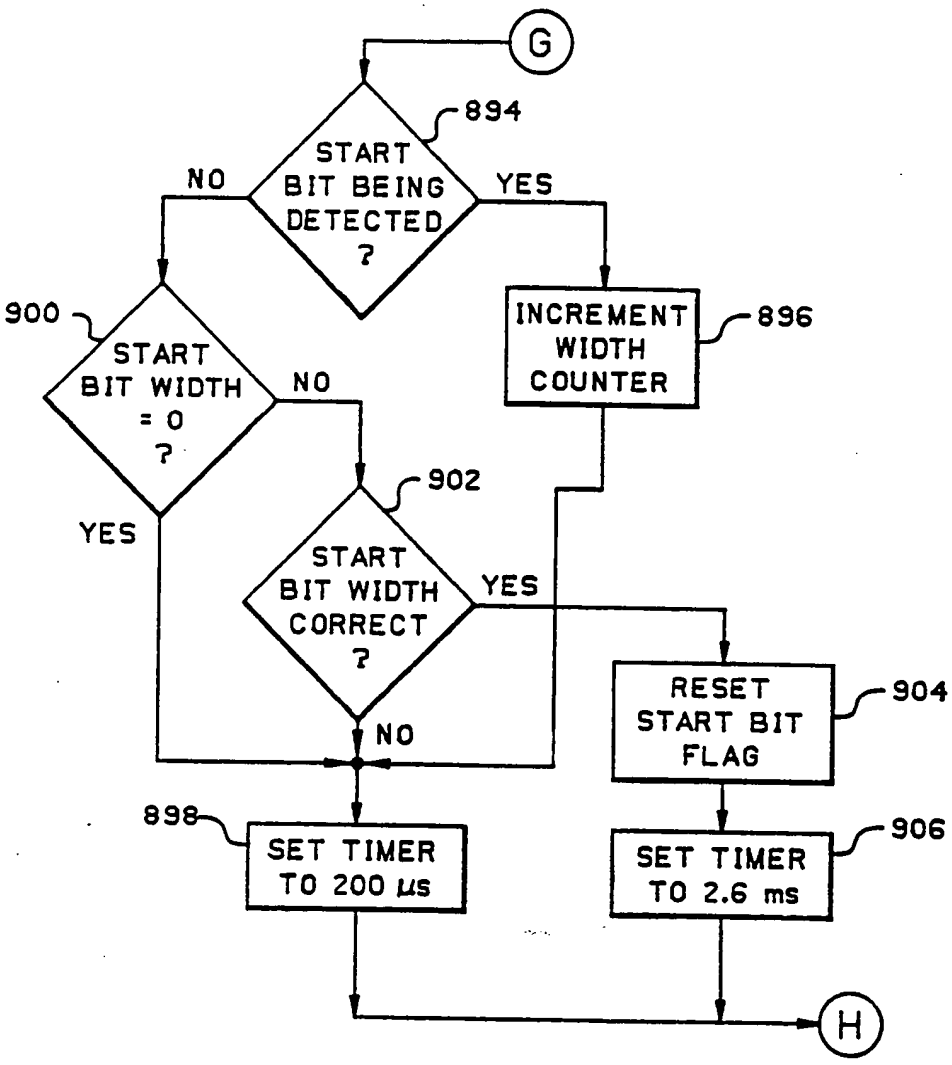

G
894
START BIT BEING DETECTED ?
NO
YES
900
START BIT WIDTH = 0 ?
NO
YES
INCREMENT WIDTH COUNTER
896
902
START BIT WIDTH CORRECT ?
YES
NO
RESET START BIT FLAG
904
898
SET TIMER TO 200 μs
SET TIMER TO 2.6 ms
906
H

FIG. 27A.

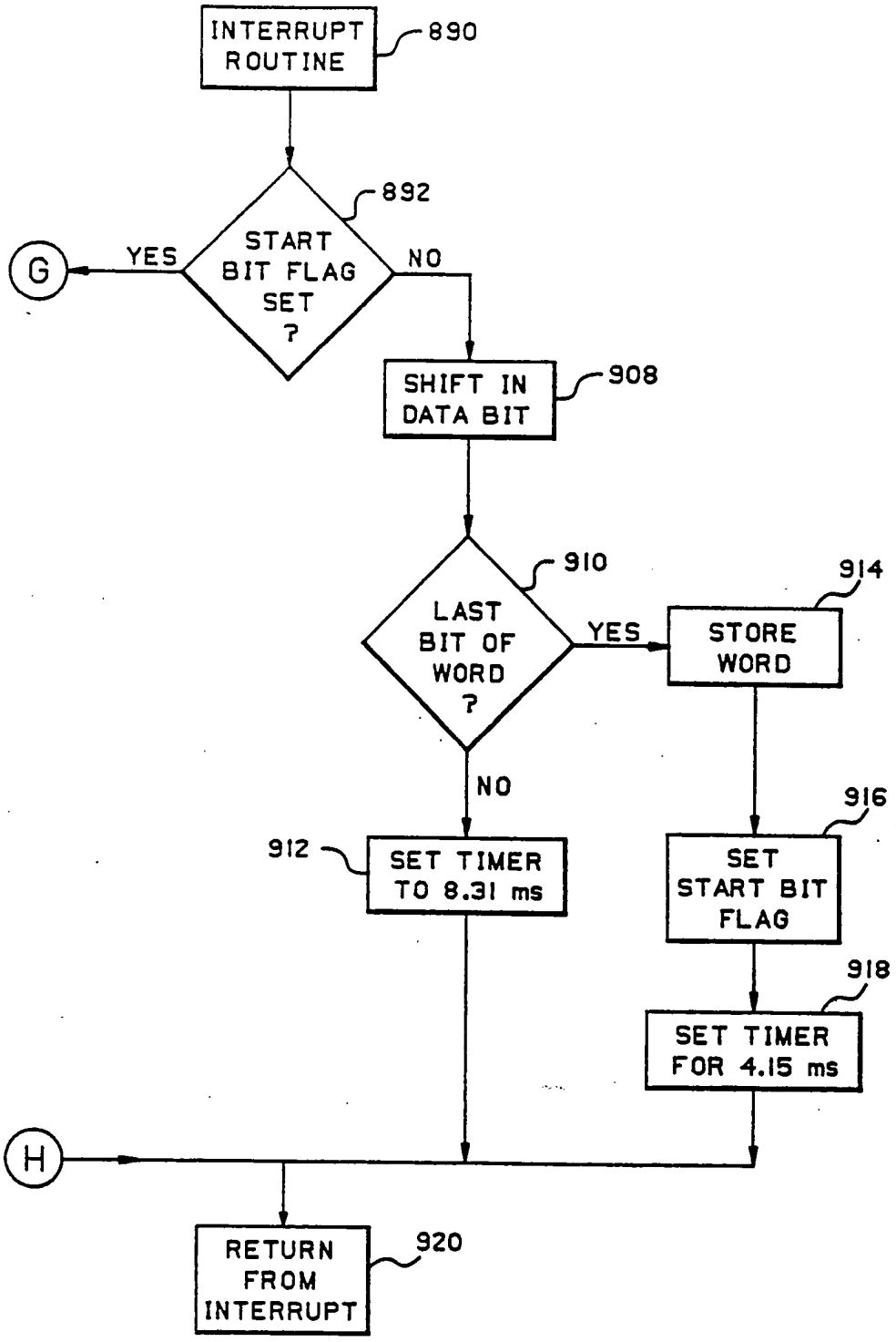

INTERRUPT ROUTINE
890
892
START BIT FLAG SET ?
YES
NO
G
SHIFT IN DATA BIT
908
910
LAST BIT OF WORD ?
YES
914
STORE WORD
NO
916
912
SET TIMER TO 8.31 ms
SET START BIT FLAG
918
SET TIMER FOR 4.15 ms
H
RETURN FROM INTERRUPT
920

FIG. 27B.

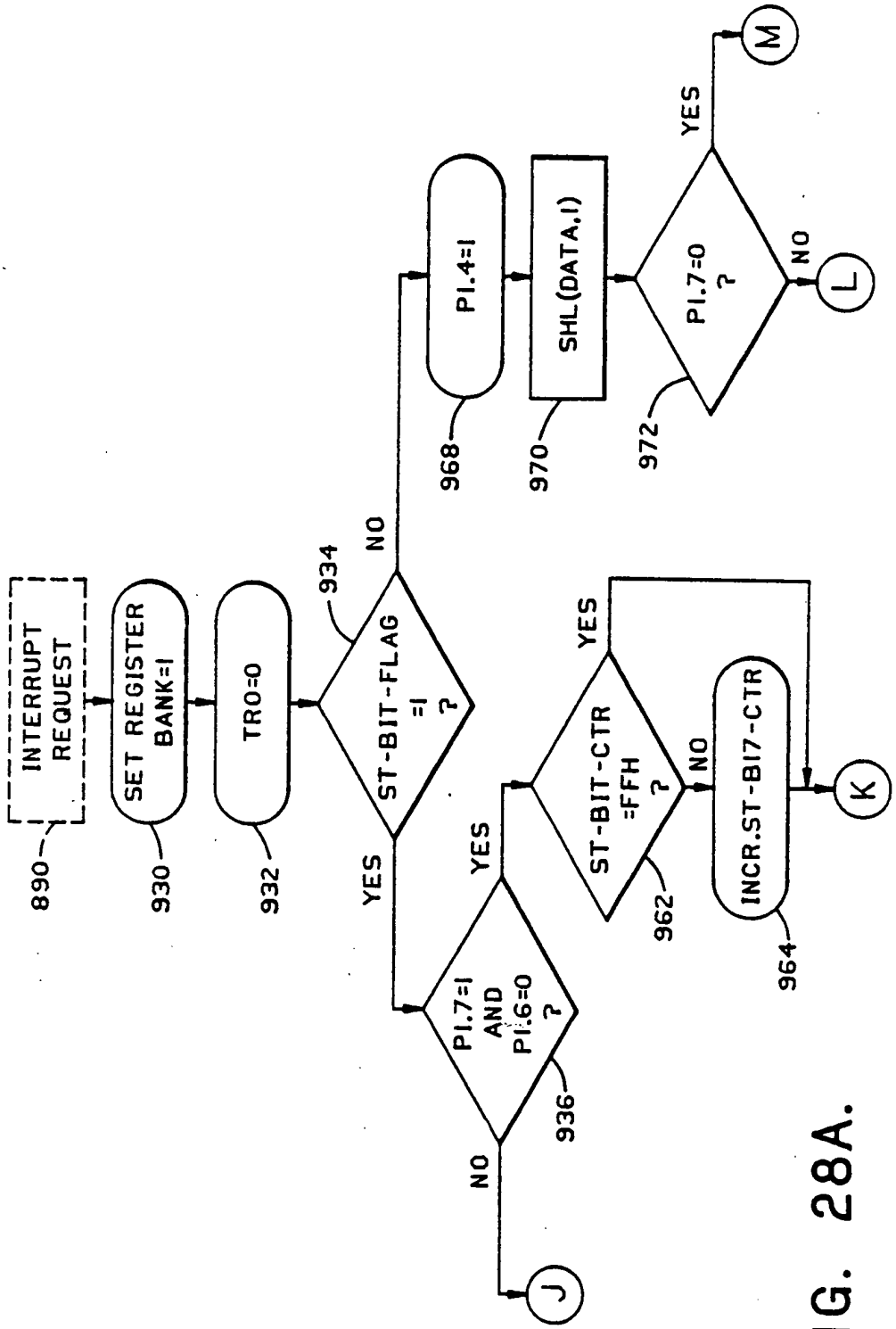
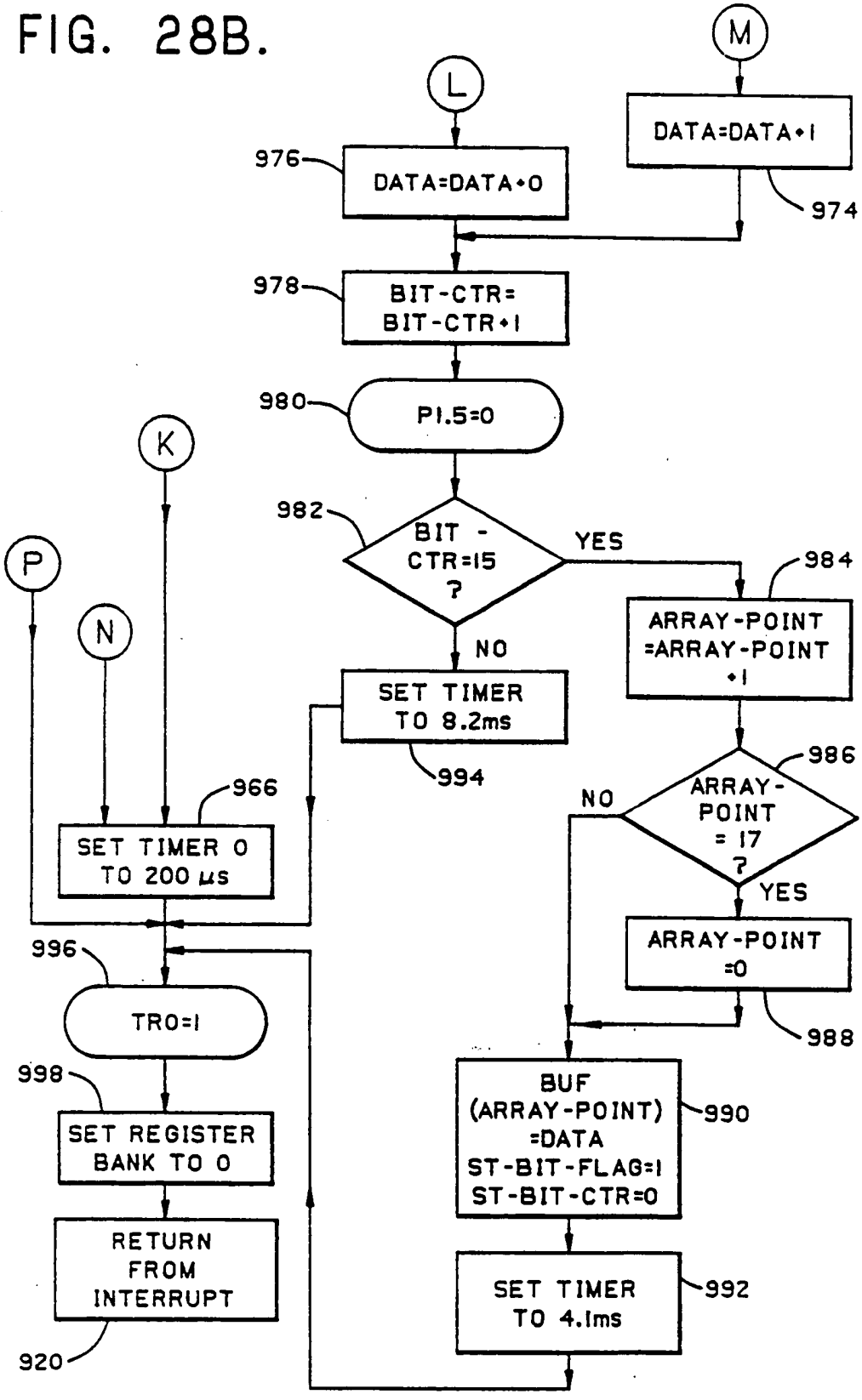

INTERRUPT REQUEST
890
SET REGISTER BANK=1
930
TR0=0
932
ST-BIT-FLAG =1 ?
934
NO
YES
P1.4=1
968
SHL(DATA,1)
970
P1.7=0 ?
972
YES
NO
M
L
P1.7=1 AND P1.6=0 ?
936
YES
NO
J
ST-BIT-CTR =FFH ?
962
YES
NO
INCR.ST-BIT-CTR
964
K

FIG. 28A.

FIG. 28B.


M
L
DATA=DATA+1
976
DATA=DATA+0
974
978
BIT-CTR=
BIT-CTR+1
980
P1.5=0
K
982
BIT -
CTR=15
?
YES
984
ARRAY-POINT
=ARRAY-POINT
+1
P
N
NO
SET TIMER
TO 8.2ms
994
986
966
NO
ARRAY-
POINT
= 17
?
SET TIMER 0
TO 200 μs
YES
996
ARRAY-POINT
=0
TR0=1
988
998
BUF
(ARRAY-POINT)
=DATA
ST-BIT-FLAG=1
ST-BIT-CTR=0
990
SET REGISTER
BANK TO 0
RETURN
FROM
INTERRUPT
SET TIMER
TO 4.1ms
992
920

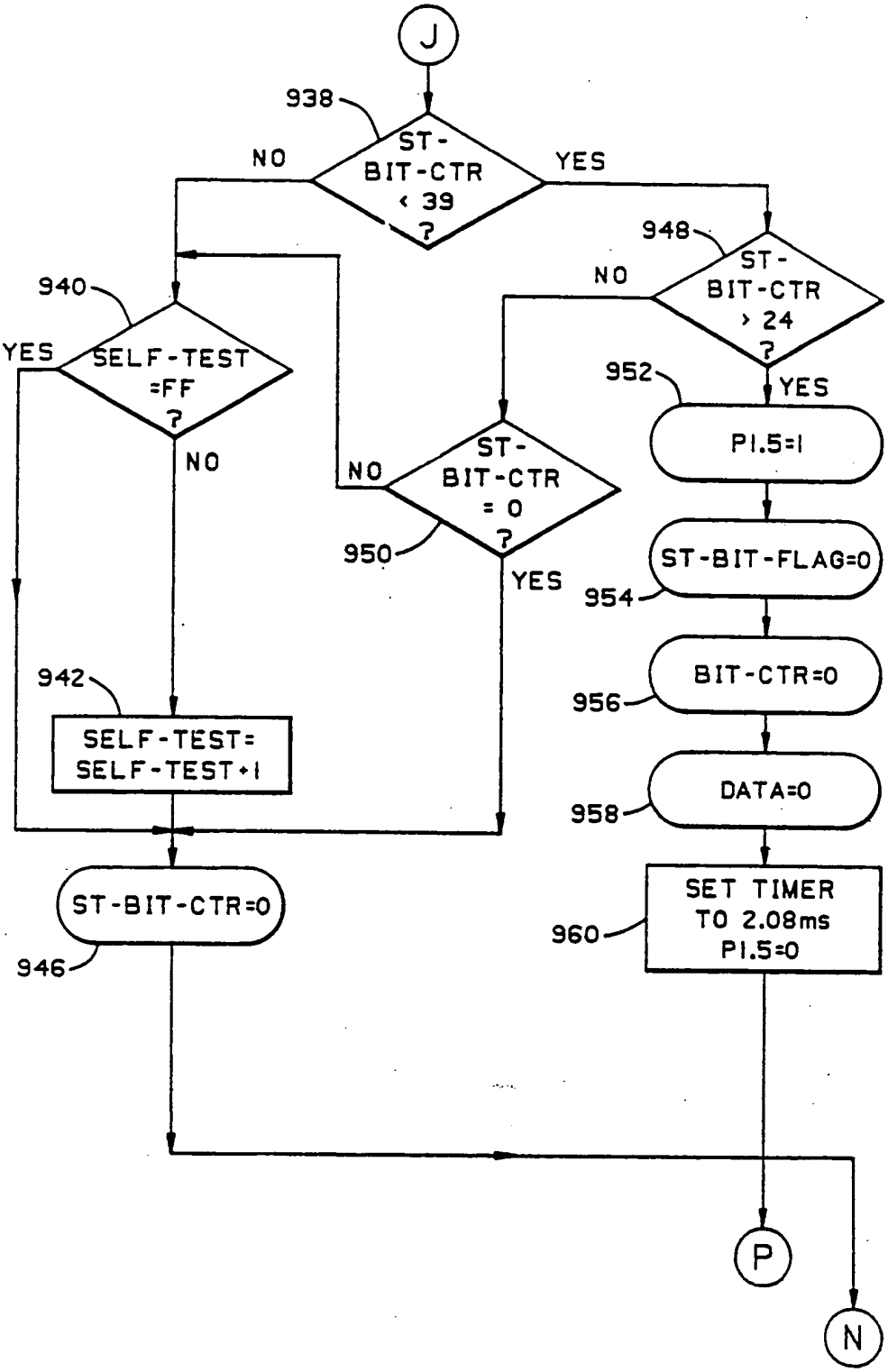

J
938
ST-BIT-CTR < 39 ?
NO
YES
948
ST-BIT-CTR > 24 ?
NO
YES
940
SELF-TEST =FF ?
YES
NO
952
P1.5=1
NO
ST-BIT-CTR = 0 ?
950
YES
954
ST-BIT-FLAG=0
942
SELF-TEST= SELF-TEST+1
956
BIT-CTR=0
958
DATA=0
ST-BIT-CTR=0
946
960
SET TIMER TO 2.08ms P1.5=0
P
N

FIG. 28C.